EE462L, Power Electronics

Lab Documents

Fall 2010

Prof. Mack Grady
Dept. of Electrical & Computer Engineering
U.T. Austin

Professor: W. Mack Grady, ENS348, 471-5231, grady@mail.utexas.edu, www.ece.utexas.edu/~grady

Office Hours: Dr. Grady's office hours for this course are Mon. and Wed 3–4, and Fri. 11–Noon. And, he is often in the power lab during the scheduled lab sessions.

Course Web Page: Linked to http://users.ece.utexas.edu/~grady/ under "Course Materials."

Reference Textbook (recommended, but not required): N. Mohan, T. M. Undeland, W. P. Robbins, Power Electronics: Converters, Applications, and Design, Third Edition, John Wiley & Sons, Inc., 2003.

Description: Analysis, design, and operation of power electronic circuits. Emphasis on single-phase power conversion from AC to DC, DC to DC, DC to AC, and maximizing the power from photovoltaics (PV). Design and construction of 150W power electronic circuits in the power laboratory, and comparison of their performance to theory. A working circuit model will be available for observation, study, and improvement. Parts and tools are provided. Use of the ECE machine shop is not required, but those of you who want to use the shop are welcome to do so. But to use the shop, you must first be "machine shop certified." See ECE technicians Paul Landers or Daryl Goodnight about shop certification and use.

Class, Lab Sessions, and Work Schedules:
- Lectures on MWF 2–3, in ENS115.
- Lab sessions in the power lab, ENS212:
    Sections 16705 and 17050, Thurs. 9:30–12:30; Sections 16710 and 17055, Thurs. 3:30–6:30, Sections 16715 and 17060, Wed. 7–10pm.
- **Always use safety glasses when soldering or drilling**.
- Never drill on the lab tables – instead, use the drill boxes or black cabinet tops (with a piece of scrap wood between your work and the table top).
- If you solder on the lab tables, keep a piece of scrap wood between your work and the table top.
- The group lab session times shown above are not sufficient to complete your projects. Work with your assigned partner for that project to meet other times as needed during the regular 2nd floor ENS undergraduate teaching lab hours.
- If you have a highly constrained schedule (work hours, sports, Longhorn band, etc.) that will make it difficult to coordinate work times with a partner, or if there are good reasons that you should work by yourself, discuss with Dr. Grady the possibility of being a solo student (i.e., no partner) for the semester.
- Regarding conduct, students should be on-time, and conduct themselves in a manner consistent with a professional environment.
- No cell phones and laptops in class. Laptops are OK in the lab. No food or drinks in class or lab.

Prerequisites: EE438 or EE331 with a grade of at least C.

Laboratory Projects: Read the lab document before starting to build! Projects are typically one-week long and require the building and testing of a circuit, and the writing of a report. Projects begin and end during the group lab sessions, according to unique section number. In addition to the group lab sessions, you should plan to work as needed during the regular 2nd floor ENS undergraduate teaching lab hours. For most projects, two-person teams are randomly assigned, with several rotations during the semester. Special requests for partners will be considered but not guaranteed. Solo requests will also be considered. If a section has an odd-number of students, then graduate students may be assigned to solo.

When due, you will turn in your hardcopy report and circuit in team order. Print your names and team number on the top of your circuit. Circuits must be in good working condition. If there is any question about circuit condition, you will be asked to demonstrate your circuit. **Messy circuits will not get credit**.

When new teams are assigned, lockers are usually swapped. The exiting team will present their tools to Dr. Grady and the TAs for checking. Teams are responsible for missing or damaged tools.

Teamwork: You are expected to work with your assigned partner as a team, splitting the work equally. The parts belong to you both. Do not do the project by yourself, leaving your partner out of the loop, unless you have cleared it with Dr. Grady and have a very good reason. Otherwise, you will receive no credit. For some projects, partner requests will be entertained. Partners must be in the same lab section.

Reports: Each project culminates in a working circuit and a written report. Without a working circuit, there can be no report. Reports (hardcopy only, no electronic) should be single-spaced and no longer than five pages, and stapled at the top left. Both team members receive the same project grade. Sample reports (pdf) are on the web page. Reports and circuits are due at the beginning of lab sessions. You are encouraged to prepare your reports in the IEEE Power and Energy Society two-column technical paper format (see the web page).

Reports are scored with fractional letter grades (e.g., A+, A, A–, etc.). The grading criteria are 1. introduction, 2. description of results (including graphs and waveforms) and any problems encountered, 3. observations, 4. neatness, and 5. conclusions. Explain what you learned in the conclusions. Compare theory to actual results.

Tests and the Final Exam: These cover mostly the theory behind the circuits, and to a lesser extent the lab procedures. You must always show sufficient work to justify your answers. When used, multiple choice questions usually have a provision for "other" answers. Grades for each test and the final exam are typically curved so that each has approximately the same average. There are no makeup tests, but if it works to your advantage, your lowest test (including a missed test) will be replaced with your final exam grade. Please do not ask to reschedule the final exam – the time and date are set university-wide. **Tests from previous semesters are found on the web page. Be smart – study the old tests and practice working out the results throughout the week before a test!**

If you have any questions about the grading of your test, follow this procedure: write down your concerns on a sheet of paper, staple it to your test, highlight on your test with a colored pen as needed to support your case, and return the stapled pack to Dr. Grady within one week.

Laboratory Safety and Equipment: You are expected to take good care of the equipment in the power lab and of the tools with which you are provided. Be a good citizen in the lab, and clean up your messes. Power labs are unlike other labs that you have taken – the voltages are higher. In some cases you will be working with hazardous voltages over 100V. Furthermore, short circuit currents can easily exceed 50A, and significant arcing can occur. Thus, it is important for you to follow the safety procedures explained by Dr. Grady and the TAs. Take off hand jewelry, watches, dangling neckchains, etc. When soldering, use safety glasses! This is especially important when "unsoldering," because when an unsoldered piece pops loose, it can "spashback" hot solder into your eyes. In power labs, you never check out your wiring by simply energizing your circuit and "hoping for the best!" Triple-check your circuit wiring, with your partner, before energizing. Finally, remember to wash your hands after soldering because solder contains lead.

Attendance: Students initial a sign-in sheet at the beginning of each class.

Grading Formula: Lab circuits and reports ---50%
Three tests ---25%
 Note – one 8.5 by 11" sheet of notes is permitted at each test and at the final exam.
Comprehensive final exam (during the official U.T. schedule) ---------------15%
Attendance and lab citizenship --10%

Group Lab Session Procedure: When a project is due, each team turns in their report (hardcopy only) and circuit when called, in team order. Be prepared to personally demonstrate your circuit to either Dr. Grady or a TA for an "Accept" or "Reject" quality check inspection of performance and construction. If the report is not ready when called, a penalty will be assessed.

Lockers, Locks, and Parts: Our 48 lockers are the only square lockers on 2nd floor. They are on the north corridor. Lockers are assigned as follows: Team #247 gets locker 247, and so on. Combination locks for lockers are randomly assigned each time partners are rotated.

All parts needed for building the circuits are provided. Most hardware, plus common parts such as screws and resistors, are kept in the power lab in the large wooden parts cabinet (southeast corner of the room) and in plastic electronic parts bin. Wire spools are mounted near the large wooden parts cabinet. Other parts are distributed at the beginning of projects.

Each team shares a tool kit (in two plastic ziplock bags, plus a static wrist band for use when handling MOSFETs. See list of tools and photos on following pages. Teams rotate lockers, but tool kits and wrist bands stay in the same lockers for the entire semester. Other tools, such as vises, are found in the power lab. Soldering irons and multimeters are obtained at the checkout counter. Students are given their own pair of safety glasses to keep with them for the entire semester.

TAs:
The main duties of the TAs are to

1. Be helpful, have a positive attitude, and treat the students as our customers.
2. Assist students by being on duty **in the lab** for approximately 10 hours per week (which includes the weekly lab sessions. (note – the first experiment requires more duty hours so that the students get off to a good start).
3. Grade the lab reports.
4. Practice with the model circuits well in advance to sharpen your proficiency in demonstrating and debugging circuits, and to make sure that you understand the circuits very well.
5. Be in charge of the weekly lab sessions, and be prepared to demonstrate the circuits and lab equipment there.
6. Help Dr. Grady in supervising the Undergraduate Assistants in keeping track of the parts inventory and wood.
7. Help Dr. Grady in supervising the Undergraduate Assistants in making sure that all lab equipment is functional and ready to go.
8. Help Dr. Grady in supervising the Undergraduate Assistants and volunteers in taking apart the circuits and salvaging the reusable parts.
9. Assist Dr. Grady in preparing the parts bags. These need to be ready-to-go one week in advance.
10. Verify early in the week that the parts bags and wood for the lab that begins on Thur/Fri are ready to go.
11. Send email updates to the course staff, alerting them of any particular problems or helpful tips.
12. Organize and oversee the end-of-semester tool, equipment, parts, and inventory wrap-up.
13. Do you job, do it well, and do it with a smile.

TAs should report for duty 4-5 days before classes start, and remain a few days after the end of classes to complete the end-of-semester tool, equipment, parts, and inventory wrap-up.

Other: U.T. policies regarding students with disabilities will be honored.

Schedule:

Week	Lecture Periods	Lab Periods
Aug. 25	Course overview. Basic circuit components.	None.
Aug. 30	SCRs, triacs, and light dimmers.	Assign Light Dimmer and Teams #I. The team writes one report, but each team member builds and demonstrates his/her own circuit. Soldering demonstration and construction tips.
Sept. 6 (Mon. is a holiday)	Transformers, diode bridge rectifiers (DBR). Waveforms and definitions.	**Light dimmer circuit and report due**. Tool check. Assign DBR and Teams #II. Rotate lockers.
Sept. 13	Photovoltaics and renewable energy. **Test #1 on Friday.**	Review DBR progress. Assign Solar and Teams #III. The solar lab does not require lockers. Do not rotate lockers.
Sept. 20	MOSFETs and MOSFET firing circuits.	**DBR circuit and report due.** Tool check. Assign MOSFET firing circuit and Teams #IV. Rotate lockers.
Sept. 27	DC-DC buck converters.	**MOSFET Firing Circuit and report due.** Assign Buck Converter and continue with Teams #IV.
Oct. 4	DC-DC boost converters.	**Buck Converter circuit and report due.** Assign Buck/Boost Converter and Teams #V. Rotate lockers.
Oct. 11	DC-DC buck/boost converters. PI controller for DC-DC boost converter. **Test #2 on Friday.**	**Buck/Boost Converter circuit and report due.** Assign PI Controller and continue with Teams #V.
Oct. 18	H-bridge inverter – basics and unipolar PWM controller.	**PI Controller circuit and report due.**
Oct. 25	H-bridge inverter – basics and unipolar PWM controller, cont.	**Solar report due**. Assign PWM Controller circuit and Teams #VI. Rotate lockers.
Nov. 1	H-bridge inverters – bridge section and output filtering.	**PWM Controller circuit and report due.** Assign H-Bridge Inverter and continue with Teams #VI.
Nov. 8	H-bridge inverter – audio amplifier.	**H-Bridge Inverter circuit and report due.** Assign Audio Amplifier and continue with Teams #VI.
Nov. 15	H-bridge inverter – renewable power to grid. **Test #3 on Friday.**	**Audio amplifier report due.** Assign Power to Grid and continue with Teams #VI.
Nov. 22	Motor drives and other applications.	Thanksgiving week. The only scheduled activity is Monday class.
Nov. 29	Course evaluation.	**Power to Grid report due.** Equipment check-in during the usual lab periods. Attendance in lab this week counts double.

Undergraduate Assistants (and their duty hours in the power lab):
    (Names pending)

The main duties of the Undergraduate Assistants and the Graduate Assistant are to:

1. **Each day,** one of them completes **List A**, replenishing the supplies as needed from the stock in the Checkout Room. When completed, List A should be signed and placed in the notebook in the TA's locking cabinet. Notify via email the entire EE362L staff upon completion, noting any shortages or issues.
2. **Each day,** same as above for **List B**.
3. **Each week**, same as above for **List C**.
4. **Each week**, same as above for **List D**.
5. When instructed, take apart the completed circuits and salvage the reusable parts. The IEEE-PES Student Chapter often provides additional volunteers.
6. Participate in the end-of-semester tool, equipment, parts, and inventory wrap-up.
7. Assist the TAs and Dr. Grady as needed.

Place each completed list at the front of the corresponding notebook tab, and keep only the two most recent lists.

For Items 1 – 4, notify Dr. Grady and the TAs via email of any shortages or problems.

List A: Daily Properly Stocked Requirements for the Power Lab
(based on 40 teams)

1. For the screw cabinet, approximately
- #8 x ½" self-tapping screws (1" deep in the drawer)
- #8 x ¾" self-tapping screws (1" deep in the drawer)
- #8 x 1" self-tapping screws (1" deep in the drawer)
- #6 x ¾" self-tapping screws (1" deep in the drawer)
- 20 of the #4-40 x 1" flat slotted nylon screws and hex nuts

- 200 of the #8-32, 1" machine screws, flat washers, split washers, and hex nuts
- 200 of the #6-32, ½" machine screws, flat washers, split washers, and hex nuts
- 200 of the #6-32, ¾" machine screws, flat washers, split washers, and hex nuts
- 200 of the #4-40 x ¾" machine screws, flat washers, split washers, and hex nuts

- 2000 of the #8, 16-14 spade terminals (about 1" deep in the drawer)
- 2000 of the #8, 22-16 spade terminals (about 1" deep in the drawer)

- 1,000 of the ¼", 22-26 quick disconnects
- 1,000 of the 3/16", 22-26 quick disconnects

- the equivalent of two full tubes of heat sink compound
- 100 of the 8" cable ties

2. For the student parts bin, approximately the number of items shown below. **Keep the 1/4W and 1/2W resistors, and the capacitors, in their plastic bags to minimize clutter and mixups**.

10Ω, 1/4W (200)
22Ω, 1/4W (200)
220Ω, 1/4W (200)
1kΩ, 1/4W (200)
1.2kΩ, 1/4W (200)
1.5kΩ, 1/4W (200)
1.8kΩ, 1/4W (200)
2.2kΩ, 1/4W (200)
3.3kΩ, 1/4W (200)
4.7kΩ, 1/4W (200)
9.53kΩ, 1/4W (200)
10kΩ, 1/4W (200)
15kΩ, 1/4W (200)
33kΩ, 1/4W (200)
47kΩ, 1/4W (200)
100kΩ, 1/4W (200)
220kΩ, 1/4W (200)
270kΩ, 1/4W (200)

1.5kΩ, 1/2W (100)
33kΩ, 1/2W (100)

0.01Ω, 3W (25)
2kΩ, 2W (50)
3.3kΩ, 1W (50)

6.8nF radial ceramic disk (100)
0.022μF radial ceramic disk (100)
0.01μF radial ceramic disk (100)
0.1μF radial ceramic disk, not dimmer (100)

5A slow-acting fuses (20)
10A fast-acting fuses (only when the H-bridge experiments are ongoing (20)

List A Continues on the Next Page

List A, Daily Properly Stocked Requirements for the Power Lab, continued
(based on 40 teams)

3. For the wire rack, the equivalent of one full spool of

- #14 black stranded
- #14 red stranded
- #14 tinned solid

- #16 black stranded
- #16 red stranded
- #16 white stranded (½ spool is OK)
- #16 blue stranded (½ spool is OK)
- #16 orange stranded (½ spool is OK)

- #22 red solid
- #22 green solid
- #22 blue solid
- #22 orange solid (½ spool is OK)
- #22 violet solid (½ spool is OK)

4. For the TA's locking cabinet
- a duplicate of the student parts bin
- two complete took kits
- two scope probes
- a multimeter
- 50 floppy diskettes and 4" x 6" 4-mil, pink plastic anti-static bags to hold them
- 10 extra 8" x 10", 6 mil plastic bags for tool kits
- a clamp-on ammeter
- 5 extra 15A fuses for the lab benches

Signed:_____

Date:_____

List B, Daily Equipment Check List
(number and condition of items in the Power Lab, along with comments as needed)

Equipment Item	Number	Comments
DC Wall Warts		(daily check – keep in 6" x 8", 6 mil, clear plastic bags)
AC Wall Warts		(daily check – keep in 6" x 8", 6 mil, clear plastic bags)
5Ω, 225W Resistor Load Banks		(daily check)
10Ω, 225W Resistor Load Banks		(daily check)
Variacs		(daily check)
Panavises		(daily check)
Drill Stations (including bits, extra batteries, chargers)		(daily check)
Lab equipment properly stored (including lost and found basket, and jumper basket)	NA	(daily check)
Lab benches		(daily check to make sure bench AC outlets have power)
TA locking cabinet in proper order	NA	(daily check)

Signed:_____

Date:_____

List C, Weekly Equipment Check List
(number and condition of items in the Power Lab, along with comments as needed)

Equipment Item	Number	Comments
3-Headlight Load Banks		(weekly continuity check)
Solar Tester Rheostats		(weekly check, no rough spots)
25V Transformer Boards		(weekly check 5A fuses)
Isolation Transformers		(weekly check)
120V, 150W Light Bulb Load Banks		(weekly continuity check)
Solar Panel Stations		(weekly check the switch, and also short circuit current)
Anti Static Mats		(weekly check the ground connections)
Installed ring static ground connecters at bench and pole outlets	NA	(weekly check for damage)
DC Wall Warts		(Weekly load check in testing circuit. Expect Vdc about 12V, Vac < a few mV)
AC Wall Warts		(Weekly load check in testing circuit. Expect both LEDs to have same brightness)

Signed:_____

Date:_____

List D, Weekly Inventory Check List for Items Stored in the Checkout Room
(number in parenthesis is the inventory to maintain, based on 40 teams)

Item	Approx. No.
#8-32, 1" machine screws (1,000)	
#8 flat washers (1,000)	
#8 split washers (1,000)	
#8-32 hex nuts (1,000)	
#6-32, ½" machine screws (1,000)	
#6-32, ¾" machine screws (1,000)	
#6-32 flat washers (1,000)	
#6-32 split washers (1,000)	
#6-32 hex nuts (1,000)	
#4-40 x ¾" machine screws (1,000)	
#4-40 flat washers (1,000)	
#4-40 split washers (1,000)	
#4-40 hex nuts (1,000)	
#8 x ½" self-tapping screws (5,000)	
#8 x ¾" self-tapping screws (5,000)	
#8 x 1" self-tapping screws (1,000)	
#6 x ¾" self-tapping screws (2,000)	
#4-40 x 1" flat slotted nylon screws (1,000)	
#4-40 nylon hex nuts (1,000)	
#8, 22-16 spade terminals (10,000)	
#8, 16-14 spade terminals (10,000)	
¼", 22-26 quick disconnects (2,000)	
3/16", 22-26 quick disconnects (2,000)	
Heat sink compound (5)	
5A slow-acting fuses (200)	
10A fast-acting fuses (200)	
15A fuses for lab benches (10)	
#14 black stranded (Two 500 foot spools)	
#14 red stranded (Two 500 foot spools)	
#14 tinned solid (Three 100 foot spools)	
#16 black stranded (Two 1,000 foot spools)	
#16 red stranded (Two 1,000 foot spools)	
#16 white stranded (Two 1,000 foot spools)	
#16 blue stranded (Two 1,000 foot spools)	
#16 orange stranded (Two 1,000 foot spools)	
#22 red solid (Two 1,000 foot spools)	
#22 green solid (Two 1,000 foot spools)	
#22 blue solid (Two 1,000 foot spools)	
#22 orange solid (Two 1,000 foot spools)	
#22 violet solid (Two 1,000 foot spools)	

Item	
9" x 12" 6-mil clear plastic bags (250) (bundled in 25's)	
8" x 10" 6-mil clear plastic bags (500) (bundled in 25's)	
6" x 8" 6-mil, clear plastic bags (1000) (bundled in 25's)	
6" x 6" 4-mil, clear plastic bags (500) (bundled in 40's)	
8" x 10" 4-mil, pink plastic anti-static bags (100) (bundled in 100's)	
4" x 6" 4-mil, pink plastic anti-static bags (500) (bundled in 50's)	

Item	
0.01Ω, 3W (200)	
10Ω, 1/4W (600)	
22Ω, 1/4W (600)	
220Ω, 1/4W (600)	
1kΩ, 1/4W (600)	
1.2kΩ, 1/4W (600)	
1.5kΩ, 1/4W (600)	
1.5kΩ, 1/2W (600)	
1.8kΩ, 1/4W (600)	
2kΩ, 2W (100)	
2.2kΩ, 1/4W (600)	
3.3kΩ, 1/4W (600)	
3.3kΩ, 1W (100)	
4.7kΩ, 1/4W (600)	
9.53kΩ, 1/4W (600)	
10kΩ, 1/4W (600)	
15kΩ, 1/4W (600)	
33kΩ, 1/4W (600)	
33kΩ, 1/2W (200)	
47kΩ, 1/4W (600)	
100kΩ, 1/4W (600)	
220kΩ, 1/4W (600)	
270kΩ, 1/4W (600)	

Item	
6.8nF radial ceramic disk (200)	
0.022μF radial ceramic disk (200)	
0.01μF radial ceramic disk (400)	
0.1μF axial, for dimmer (200)	
0.1μF radial ceramic disk, not dimmer (600)	

Item	
8" cable ties (400)	

Item	
1" x 6" wood, 7" long pieces (50)	
1" x 6" wood, 10" long pieces (150)	
1" x 6" wood, 12" long pieces (100)	
1" x 10" wood, 16" long pieces (50)	

Signed:_____

Date:_____

Tools:

Tool Kit #1, Pliers and Wire Strippers (7 items)

- Crimping and stripping tool, red 3M TH-440 (Mouser #517-TH-440, or Grainger #4X316), or Xcelite 104CG (Mouser #578-104CG). Two of these.
- Long nose pliers with cutter, 6" blue Channellock #326 (Lowe's Home Improvement, or Grainger #3LY70)
- Slipjoint pliers with cutter, 6" blue Channellock #526 (Lowe's Home Improvement, or Grainger #3LY75)
- Diagonal cutting pliers, 4 and ½" 1/2 green Utica U463, or 5" green Xcelite S475JS (Mouser #578-S475JS)
- Wire strippers with (or without) spring and cam adjustment, DES Tools (Mouser #5876-103S or #5876-100)

Tool Kit #2, Screwdrivers and IC Extractor (7 items). Two of these.

- 8&1/8", Phillips #2, yellow, Xcelite X102 (Mouser #578-X102)
- 3" slotted, 3/16" wide, black and yellow, Stanley 66-015 (Grainger #6C251)
- 3" slotted, 5/32" wide, yellow, Xcelite R5323 (Newark #34F259)
- 3" slotted, 1/8" wide, red, Xcelite R183 (Mouser #578-R183)
- Trimmer potentiometer adjustment tool, Vishay/Spectrol (Mouser #594-8T000)
- IC extractor tool, spring steel (Mouser #524-9227)

Tool Kit #1 (has **two** of the large crimping and stripping tools)

Please keep Tool Kits #1 and #2 grouped as shown in their reclosable bags
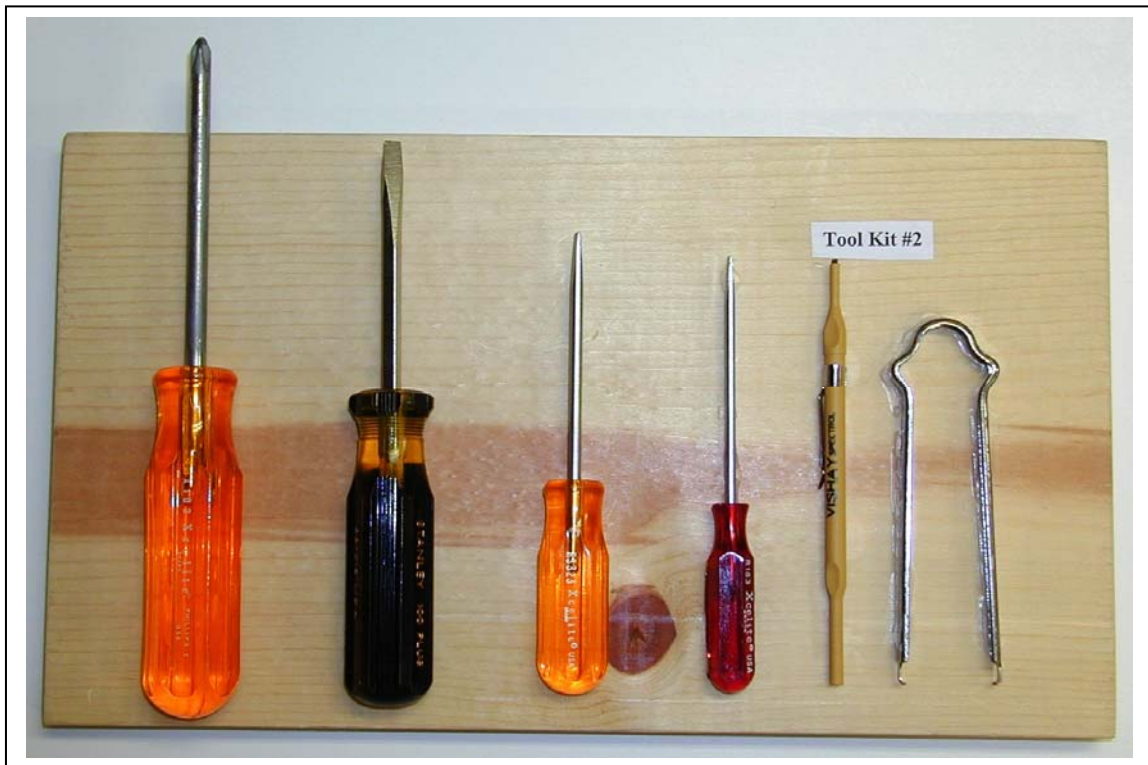
Tool Kit #2 (has **two** of the large Phillips screwdrivers)
To prevent damage to screwdriver tips, always use the largest screwdriver that fits the screw.

Additional Tools: Safety Glasses (each student keeps theirs) and Static Wristband (one per team)
Please keep the safety glasses and static wristband in their individual reclosable bags or boxes. The safety glasses' lenses are easily scratched if bagged with tools.
(Safety glasses (over glasses type), UVEX S0112, Grainger #6T359)
(Static wristband with 6' coil cord, SPI-Westek 95113, Mouser #809-SP106B-B6)

Additional Tool: Oscilloscope Probe (Agilent 10074C 10:1) in Anti-Static Bag
(Your tool kit has one probe. Additional probes are available at the check-out window.)

Other Stock Equipment and Tools: Stock equipment and tools that you will use regularly include
- 120V input, 0-140V output, 1.4kVA, 10A variable autotransformers (Superior Electric POWERSTAT L2M116C, Newark #91F5311)
- Oscilloscopes (Agilent 54621A, 60MHz)
- Vises (Panavise Standard 301, Mouser #591-301, or Jr. Mini 201, Mouser #591-201)
- 115V/115V, 500VA line isolation transformers (Hammond 171E, Newark #96F5547)
- Two portable hand drills and 3/32" bits for drilling starter holes in wood. Use the drill boxes so you do not accidentally drill into a lab bench of table.
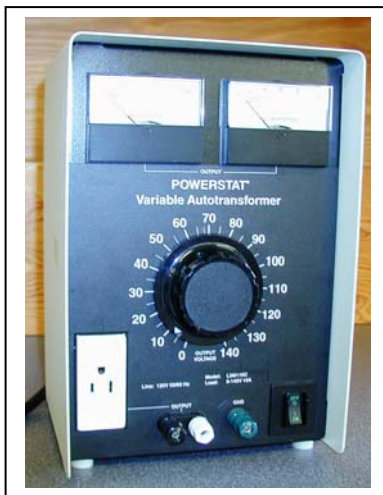
Variac   Isolation Transformer
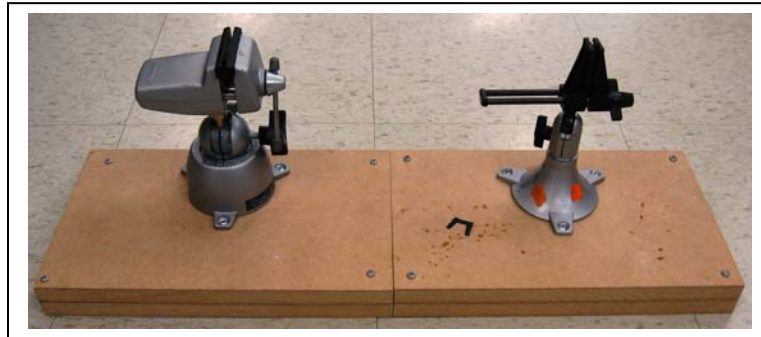
You will also use two other pieces of equipment that were assembled especially for this course. These are 120/25V, 250VA transformers mounted on boards (Hammond 165S25, Newark #92F1340), and three series automobile headlights as load banks. Both are shown below. The plastic electrical switch box to the left of the transformer contains a toggle switch, 5A "slow blow" fuse, fuse holder (Bussmann #HJM, Newark #27F819), and neon indicator light (LC&D #75R-2211T, Newark #16F736).
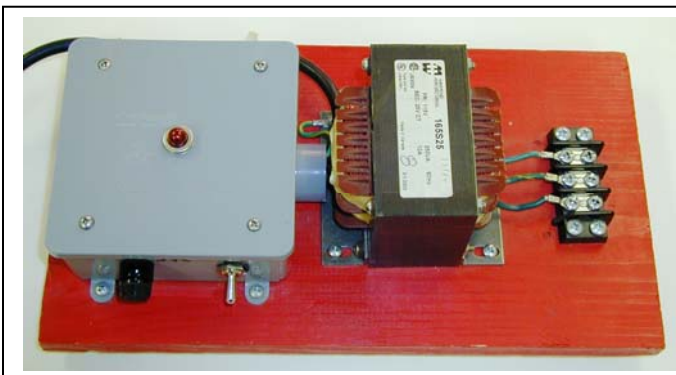
120/25V Transformer Board

Three Series Headlight Load Bank

Special Generous Donation: Schweitzer Engineering Labs donated more than thirty SEL-421s for our power engineering laboratory. In EE362L, they are used as voltmeters/ammeters/wattmeters and as waveform capture devices.

Schweitzer Engineering Labs SEL-421 Relay
(the SEL-421 also serves as three-phase meter and event-triggered waveform capture device)

We power the SEL-421s through in-line ground fault interrupters (Hubbell GFP2CA).
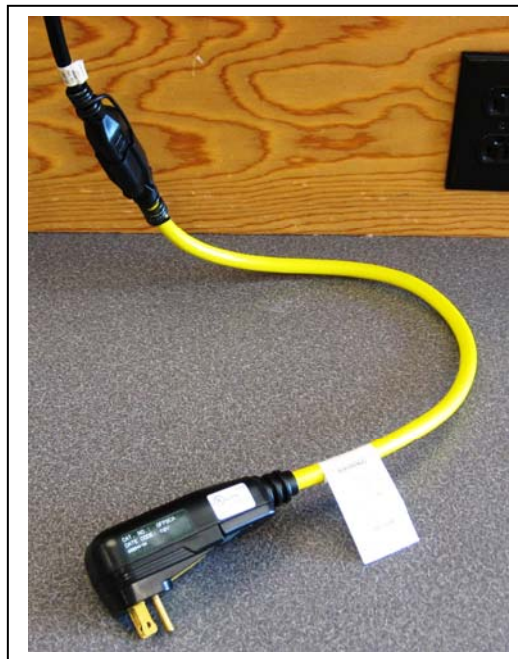
Plastic Bags: Reclosable plastic bags (Minigrip from Consolidated Plastics, www.consolidatedplastics.com) are essential. They are
- 9" x 12", 6 mil clear plastic for large items or circuit parts
- 8" x 10", 6 mil, clear plastic for tools or circuit parts
- 8" x 10", 4 mil, pink plastic anti-static for scope probes
- 6" x 8", 6 mil, clear plastic for circuit parts, wall warts, or safety glasses
- 6" x 6", 4 mil, clear plastic for circuit parts
- 4" x 6", 4 mil, pink plastic anti-static for sensitive components, anti-static wristbands, and floppy diskettes.

Suggestions for Improvements: Your suggestions for improving the course will be greatly appreciated. Many improvements have been made thanks to students from previous semesters. Consider the following:

- Do you have ideas for improving the experiments?
- Are there errors or clarifications needed in the lab documents?
- Should any of the experiments be deleted? If so, which ones?
- Should new experiments be added? If so, what topics?
- Do you see ways to increase your efficiency in completing the experiments (tools, equipment, supplies and parts, bench scheduling, storage, partner assignment, lockers, etc.)

Project Wood:

Project wood should be of good quality and not warped (and not likely to warp) so that the pieces lie flat on a table without wobbling. The pieces needed for 40 teams are:

Cut from 1" x 6" lumber
- 150 pieces, 10" long (need by week #1)
- 100 pieces, 12" long (need by week #2)
- 50 pieces, 7" long (need by week #4)

Cut from 1" x 10" lumber
- 50 pieces, 16" long (need by week #8)

In the past, we have used choice lumber, or birch, from Lowe's or Home Depot. It is often soft enough that the students can drive wood screws in by hand. For harder wood pieces, use a drill to make starter holes.

The photo below shows a typical project.

Circuit Tear-Down and Salvaging

After judging, non-ribbon winning teams are expected to salvage their circuits. DBRs are an exception – half are kept in service throughout the semester. Salvaging is a requirement to receive a lab grade for a circuit. Some parts are re-used if they are in good condition. Other items are placed in surplus in ENS212. Only high-quality parts are re-used. Undamaged wood screws and machine screws without heat sink compound on them should be returned to the wooden screw cabinet. Most of the wood is kept for general student use.

Here are details, circuit by circuit. Put the parts shown below in the plastic bags as they were initially distributed, **with your names visible on a piece of paper inside the bag so you will receive lab credit**.

Light Dimmer (the following go back in bags as you received them, with your names visible inside)

Item	Re-Use	Salvage	Comments
60W Light Bulbs	•		Ohm check. Individually pack in 6x8", 6 mil plastic bags.
Porcelain Light Bulb Bases	•		Snug the screws. If there are any missing screws, see Dr. Grady of a TA for spares. Individually pack in 6" x 8", 6 mil plastic bags.
Corner Brackets	•		Cleaned
Terminal blocks	•		Snug the screws. If there are any missing screws (except the red-marked hole), see Dr. Grady of a TA for spares.
Rubber Washers	•		
Triacs		•	Cut off the wires, just beyond the triac leads
Potentiometer & Lock Nut		•	Cut off the wires. Put the lock nut back on the pot.
Small Heat Sinks		•	

DBR (the following go back in bags as you received them, with your names visible inside). Half are salvaged right away, and the other half are salvaged at the end of the semester.

Item	Re-Use	Salvage	
Large Heat Sink	•		Cleaned
DBR Module	•		Cleaned. Quick disconnects removed.
Corner Brackets	•		Cleaned
Terminal Blocks	•		Snug the screws. If there are any missing screws, see Dr. Grady of a TA for spares.
Capacitor	•		Note for staff – these will be used for four semesters, then salvaged. When finishing a semester, write the semester, e.g. Fall 08, on the side with a permanent marker. If suspect for damage (i.e., bulging, pop-off valve extended, etc.), mark an "X" on the side with a permanent marker and discard.
Capacitor Clamp	•		
Wooden Clothes Pin	•		
Toggle Switch & Lock Nut		•	Remove from bracket, pull off quick disconnects, and put the lock nut back on the toggle switch
Thermistor		•	
LED		•	Cut off the wires, just beyond the LED leads
0.01Ω Resistors		•	Leave spade connectors on

MOSFET Firing Circuit (the following go back in bags as you received them, with your names visible inside). These are salvaged at the same time as the DC-DC converters.

Item	Re-Use	Salvage	
Large Heat Sink	•		Cleaned
Corner Brackets	•		Cleaned
Terminal Blocks	•		Snug the screws. If there are any missing screws (except the orange-marked hole), see Dr. Grady of a TA for spares.
MOSFET and Green Plug		•	Remove from terminal block, but leave #14 solid wires and 100kΩ resistor attached. Cleaned.
Protoboard		•	All parts removed
Chips		•	Keep in sockets
Wall Wart Jack		•	Cut off the wires and ceramic capacitor
Snap-in Potentiometers		•	
Ceramic Capacitors		•	

DC-DC Converter (the following go back in bags as you received them, with your names visible inside)

Item	Re-Use	Salvage	
Corner Brackets	•		Cleaned
Terminal Blocks	•		Snug the screws. If there are any missing screws, see Dr. Grady of a TA for spares.
Red 33μF Capacitor	•		Leave spade connectors on. These capacitors will not be re-used if the leads are badly bent.
Black 100μH Inductors on Heat Sinks		•	Assembly intact with nylon screw and nut
Rectifier and Heat Sink		•	Assembly intact. Wires cut off just beyond the rectifier leads.
Output Capacitor (black)		•	Leave wires and spade connectors attached
Red 10μF Capacitor		•	Leave spade connectors on
0.01Ω Resistor		•	Leave spade connectors on

Inverter (the following go back in bags as you received them, with your names visible inside)

Item	Re-Use	Salvage	
Corner Brackets	•		Cleaned
Terminal Blocks	•		Snug the screws. If there are any missing screws, see Dr. Grady of a TA for spares.
DC-DC Converter Chips	•		Keep in sockets. Note to staff – these need to be load checked for DC voltage and AC ripple voltage at the end of the semester.
Triangle Wave Generator	•		Keep in socket. Note to staff – these need to be waveform checked at the end of the semester.
Fuse Blocks	•		Remove fuses and quick disconnects
Heat Sinks	•		Cleaned
Red 100µH Inductor	•		Leave spade connectors on
Protoboards		•	All parts removed
MOSFETs and Green Plugs		•	Remove from terminal blocks, but leave #14 solid wires and 100kΩ resistors attached. Cleaned.
Chips (Other Than DC-DC Converters and Triangle Wave Generator)		•	Keep in sockets
Red 10µF Capacitors		•	Leave spade connectors on
Wall Wart Jacks		•	Cut off the wires and capacitors
Potentiometers		•	For the wire-wound, cut off the wires and put the lock nut back on the pot.
Ceramic Capacitors		•	

End-of-Semester Parts, Tools, Equipment, and Inventory Wrap-Up:

1. Complete Lists A, B, C, and D.

2. Screwdrivers – check for damage, e.g., twisted shafts in the small screwdrivers, and worn tips in the larger screwdrivers. Clean, count, and bag the good ones by type for re-use. Else, brand, bag, and put in the surplus cabinets.

3. Large and small wire strippers – check for those that do not strip properly or have too much play in the joint. Clean, count, and bag the good ones by type for re-use. Else, brand, bag by type, and put in the surplus cabinets.

4. Diagonal cutting pliers and long nose pliers – check for cutting edge damage, or stiffness. Clean, count, and bag the good ones by type for re-use. Else, brand, bag by type, and put in the surplus cabinets.

5. Static wrist bands – If undamaged and not too worn, pack in new pink bags, and count for re-use. Else, discard.

6. Scope probes – check calibration. Check alligator ground by observing the 60Hz voltage waveform of one of the 25V transformers. If OK, pack in new pink bags. Else, ask Daryl or Paul to inspect it.

7. Put jumpers that are in good condition, with soldered terminals on both ends, into a jumper basket. Else, discard.

8. Keep 15-20 good wood pieces if each size, that can be used on the flip side. Discard all others.

9. Safety glasses and floppy diskettes not kept by the students should be put in the surplus cabinets.

List E: Other Inventory Items To Be Fully Stocked at Semester Start

(stored in Checkout Room (CR), or in ENS624B)

Item	Actual No.
Tool kits #1 (in CR)	
Tool kits #2 (in CR)	
Safety glasses (in CR)	
Static wristbands (in CR)	
Oscilloscope probes (in CR)	
Light dimmer kits (in CR)	
DBR kits (in CR)	
MOSFET Firing Circuit kits (in CR)	
Buck Converter kits (in CR)	
Buck/Boost Converter kits (in CR)	
Inverter Control Circuit kits (in CR)	
Inverter Isolated Firing Circuit kits (in CR)	
Inverter H-Bridge kits (in CR)	

Item	Actual No.
Steel corner brackets, 1" drilled special (in 624B)	
Steel corner brackets, 1½" (in 624B)	
Steel corner brackets, 2" (in 624B)	
Steel corner brackets, 2" drilled special (in 624B)	
DC jacks (in 624B)	
Green plugs (in 624B)	
Protoboards, EXP350, 3.6" (in 624B)	
Protoboards, EXP300, 6" (in 624B)	
Terminal blocks, 2-terminal, 30A (in 624B)	
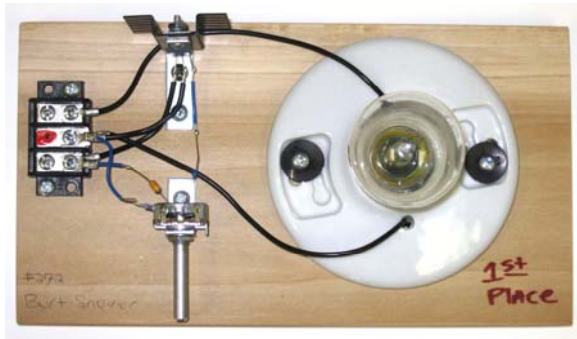
Light Dimmer
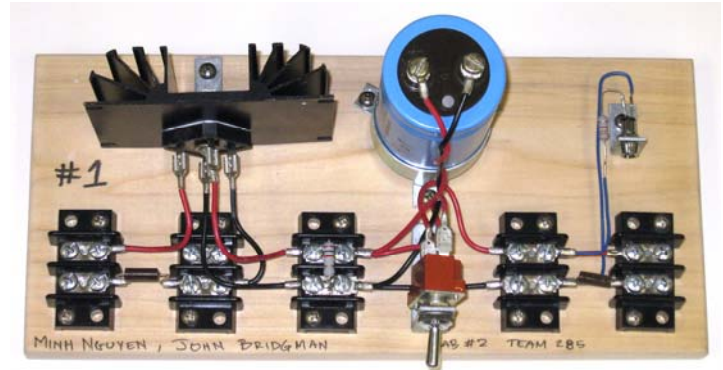
Diode Bridge Rectifier
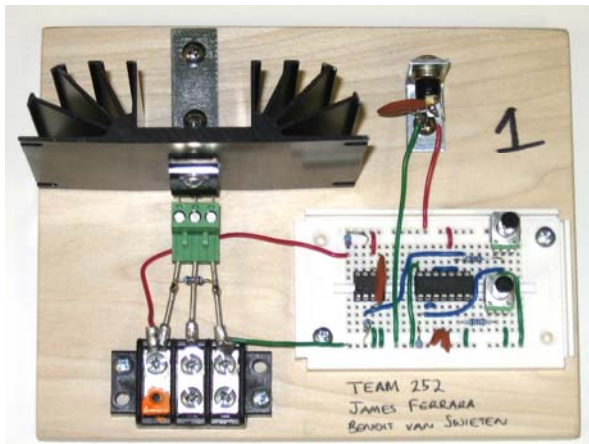
MOSFET Firing Circuit
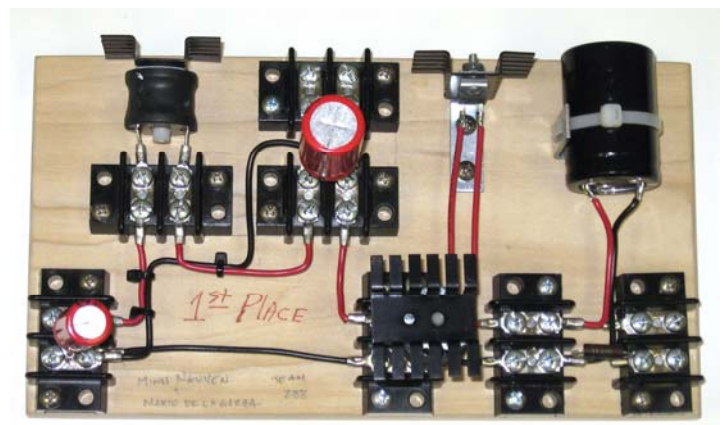
DC-DC Buck/Boost Converter

Inverter

EE462L, Power Electronics, Triac Light Dimmer
Version Aug. 30, 2010
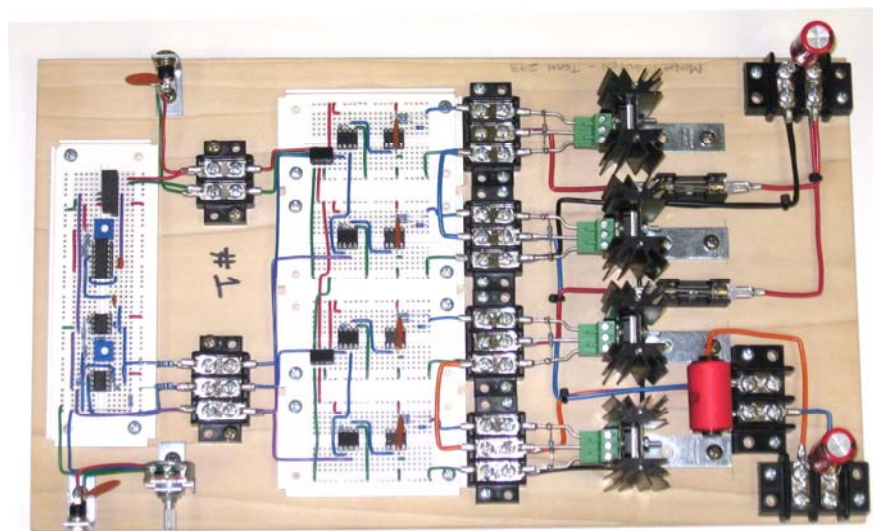
Notes before starting – Read this report carefully. Every student builds a circuit, but each team writes only one report.

Wear safety glasses when soldering or viewing an energized power circuit from a close distance. Remove watches, bracelets, rings, and dangling neckchains when performing this experiment. Do not energize your circuit without the assistance of Dr. Grady or one of the TAs. Do not mount the steel corner brackets so that they touch each other. Do not attempt to use this circuit at home with 120Vac because a serious shock may result.

All oscilloscope screen snapshots in this document serve as checkpoints – do not pass a checkpoint until your circuit has approximately the same waveform shown. Snapshots designated by the following boxes:

> Save screen
> snapshot #N

should be saved for your report.

Overview
A light dimmer regulates power flow to a resistive load, such as an incandescent light bulb, in an efficient way by allowing only a portion of the 60Hz current to pass through. Example current (and voltage) waveforms to a resistive load are shown in Figure 1 for firing angles $\alpha = 30°$, $90°$, and $150°$. Firing angle is controlled by a potentiometer, RC circuit, and diac. The variation of load power with α is shown in Figure 2.
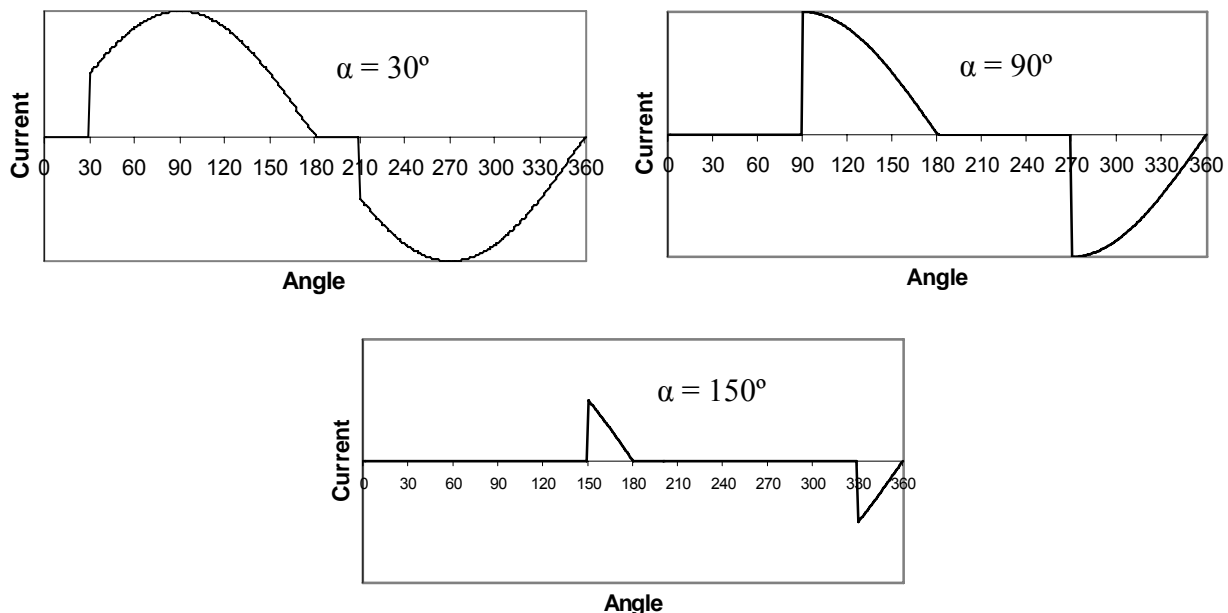
Figure 1. Resistive load current (and voltage) waveforms for firing angles
$\alpha = 30°$, $90°$, and $150°$
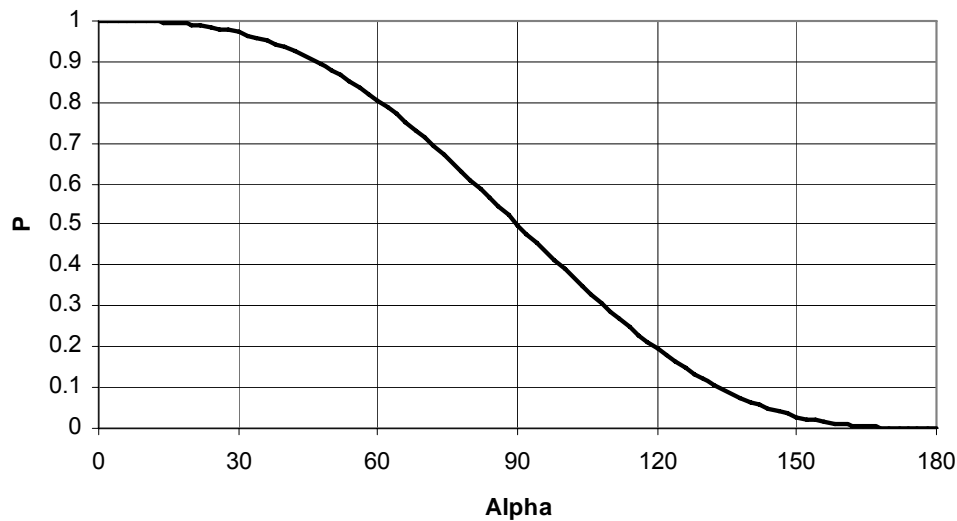
Figure 2. Normalized power delivered to resistive load versus firing angle
(this is a normalized plot of Equation (1) in the *Lab Report* section)

Two important characteristics of the light dimmer current are that 1. it has zero average value
(i.e., no DC, which minimizes corrosion of power grounds), and 2. it has half-wave symmetry
(i.e., has no even-ordered harmonics).

The light dimmer circuit that you will build is designed for use at 120Vrms. However, you will
perform your experiment with using an isolation transformer and variac set at 70Vrms.

Light dimmer circuit and operation
The light dimmer circuit is shown in Figure 3. During each half-cycle, when the voltage across
the capacitor (either positive or negative) exceeds the breakover voltage of the diac and "fires"
the triac, current then flows through the load. The RC time constant of the series 3.3kΩ + 250kΩ
linear potentiometer and 0.1µF capacitor determines the phase delay and magnitude of the
sinusoidal capacitor voltage with respect to the source voltage. Once firing occurs, the voltage
across the triac collapses, the capacitor voltage goes to nearly zero, and the entire process resets
at the beginning of the next half-cycle. For the circuit to work properly, a small current must
flow through the load before firing occurs, but this current is miniscule with respect to full load
current.

Light
bulb
a   b

Triac
(front view)

3.3kΩ

+
V_{an}
(from Variac)
−

250kΩ
linear
pot

MT2

c   G   Triac

MT1

MT1 MT2 G

0.1µF

Bilateral trigger
diode (diac)

n

Light
bulb
a   b

+   + 0V −   +
V_{an} V_{an}
−   n   −
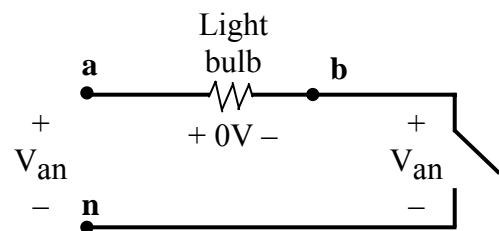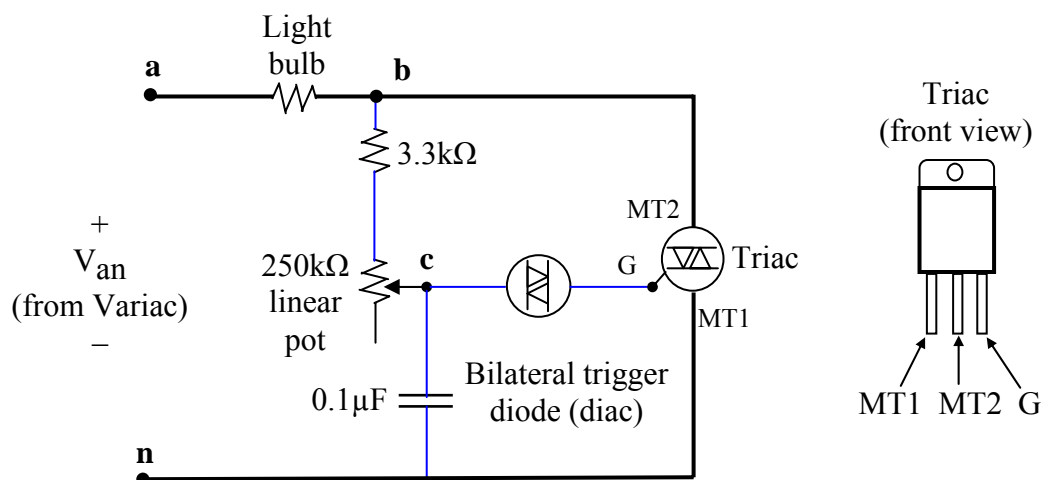
Before firing, the triac is an open switch,
so that practically no voltage is applied
across the light bulb. The small current
through the 3.3kΩ resistor is ignored in
this diagram.

Light
bulb
a   b

+   + V_{an} −   +
V_{an} 0V
−   n   −
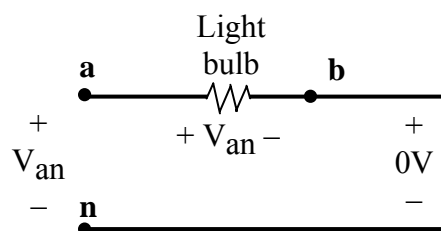
After firing, the triac is a closed
switch, so that practically all of V_{an}
is applied across the light bulb.

Note - when the potentiometer is adjusted to 0Ω, the time constant of the RC circuit (ignoring
load resistance) is $3300 \cdot 0.1 \cdot 10^{-6} = 0.330$msec, which is small compared to one-half period of
60Hz (i.e., 8.33msec). When the potentiometer is at 250kΩ, the time constant is 25.3msec,
which is relatively large.

Figure 3. Light dimmer circuit with triac
(Use blue #22 solid wire for control electronics when the leads of small electronic components
are not long enough to make connections. Current-carrying wires should be #16 stranded.)

Oscilloscope probes

Before using a probe, you should
1. calibrate it, and
2. check the integrity of its ground.

Calibration is performed by connecting the probe to the calibration terminals on the oscilloscope, and then selecting "Auto Scale." Use a trimmer potentiometer adjustment tool to turn the screw on the probe's plug until the wave is square.
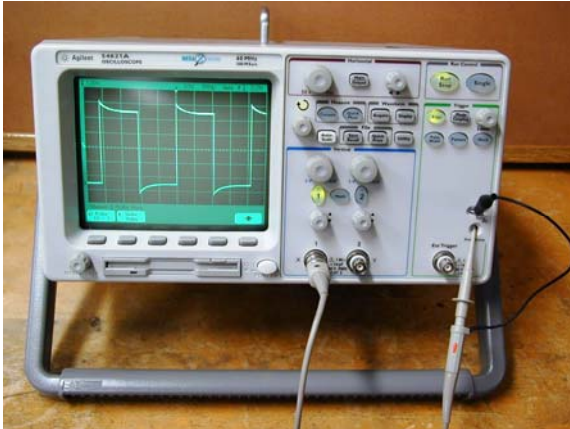
If the alligator ground clip is loose or broken, the oscilloscope trace that you see for a signal whose ground is not the same as the oscilloscope chasis will be either false or "shaky." You can prevent this problem by either checking the resistance between the alligator clip and the outside of the BNC connector, or by viewing the waveform of an ungrounded source (such as from a 25V transformer). If a probe is defective, report it to the checkout counter.
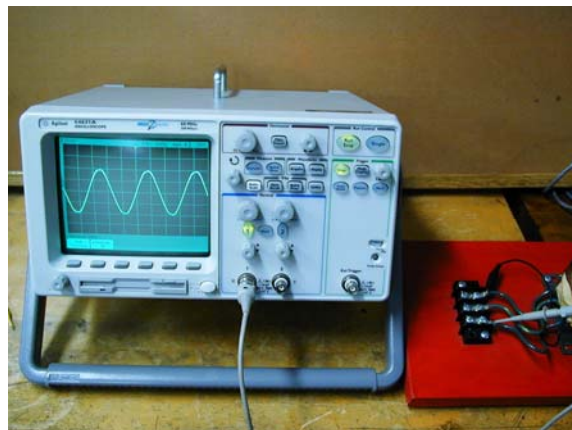
The experiment
Work at either a lab bench, or on top of one of the black cabinet tops. Never place the hot tip of a soldering iron on the surface of a lab bench or table. Instead, use the coiled wire holster. Do you soldering on a wood piece, or using a Panavise. Remember to use safety glasses.

Use #16 stranded wire for your power connections, and #22 solid wire for the control connections (i.e., potentiometer, diac, capacitor, and Triac gate wire).

Make two sets of jumper cables that you will use all semester. Cut two 3" pieces of #14 stranded copper wire from the large spools (one red piece, and one black piece), and two 6" pieces (again, one red, and one black). Crimp and solder spade connectors to both ends of each wire.

A. **Use Excel spreadsheet EE462L_Triac_Light_Dimmer.xls to predict the performance of the light dimmer circuit**
    EE462L_Triac_Light_Dimmer.xls can be run or downloaded from the class web page. Click "Enable Macros" when asked. Vary the value of the 250kΩ potentiometer using the "R potentiometer" slide bar. If macros are not permitted on your PC, then simulate potentiometer action by changing the potentiometer resistance value in the yellow cell. Triggering occurs when the capacitor voltage exceeds the diac breakover voltage.

B. **Using the parts provided, build the light dimmer circuit shown in Figure 3.**
    Note - to avoid screwing all the way through your wood piece, use #8 x ¾" self-tapping screws for the terminal block, and #8 x ½" self-tapping screws for the steel corner brackets.

    An example circuit is provided in the glass case outside Dr. Grady's office for your inspection. Use #16 black stranded wire for power connections, and #22 blue solid wire for connecting the control electronics. Minimize your use of #22 solid wire by using the leads of the devices as much as possible. **Do not use heat shrink** in your circuit (because it tends to hide the quality of your soldering!). Mount your triac so that the leads point downward. Mount your potentiometer so that turning the shaft clockwise increases light intensity. Mount the porcelain light bulb holder using a rubber washer between each #8 x 1" self-tapping screw head and the porcelain to prevent the porcelain from cracking. **After your circuit is built, write your names on the top surface of the wood.**

C. As shown in the photograph below, connect your light dimmer circuit with bulb to the isolation transformer and variac (but do not yet energize)

1. Make sure that your variac switch is "off" and that its output voltage control knob is **fully counterclockwise** (to the 0V position).

2. With the variac "off," connect your light bulb and light dimmer circuit in series with the output of the variac as shown in Figure 3. **The variac black post is "hot," and the white post is "neutral." Do not use the green post (i.e., "ground").**

3. **Plug the variac into an isolation transformer, and the isolation transformer into a wall outlet.** The isolation transformer removes the ground reference from the variac output, adding a degree of safety. **Important – do not leave the isolation transformer plugged into the wall outlet after you are finished because it will get hot!**

D. Test your circuit with V_{an} = 70Vrms and a 120V, 60W incandescent light bulb load

1. Make sure that your variac switch is "off" and that its output voltage control knob is **fully counterclockwise** (to the 0V position).
2. With the variac "off," connect your light bulb and light dimmer circuit in series with the output of the variac as shown in Figure 3. **The variac black post is "hot," and the white post is "neutral." Do not use the green post (i.e., "ground").**
3. **Plug the variac into an isolation transformer, and the isolation transformer into a wall outlet.** The isolation transformer removes the ground reference from the variac output, adding a degree of safety. **Important – do not leave the isolation transformer plugged into the wall outlet after you are finished because it will get hot!**
4. Turn your light dimmer potentiometer to the full clockwise position.
5. Turn on the variac, and slowly raise the output voltage knob to 70Vrms. The bulb should light up. Use a handheld multimeter across the black and white posts and adjust for V_{an} = 70±1 Vrms.
6. Vary your light dimmer potentiometer across its full range and observe the light bulb to verify that your circuit is controlling light bulb brightness properly.
7. Turn the variac output voltage knob to zero, and then turn off the variac switch.
8. **Remember – you must always de-energize 120V circuits before making connections or attaching oscilloscope probes!**
9. Connect an oscilloscope probe to monitor light bulb voltage V_{ab}.
10. Re-energize your circuit with V_{an} = 70Vrms, and set the potentiometer for full brightness. Display one or two cycles of V_{ab} on the oscilloscope. Use the time cursors to measure firing angle α in milliseconds, and waveform period (or half-period) in milliseconds. Convert α to degrees. Measure $V_{ab,rms}$ with a multimeter **and** with the oscilloscope. (Note – not all multimeters compute true rms for nonsinusoidal waveforms - see Step 11.) When using an oscilloscope to measure rms, be sure to adjust the time resolution so that **at least six periods of the waveform** are visible on the screen. Record $V_{ab,rms}$ (multimeter and oscilloscope), and α.
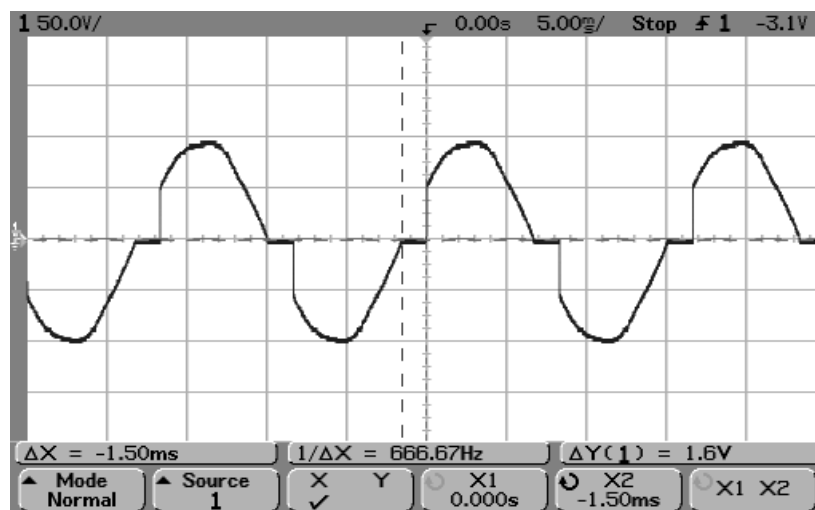
11. While viewing the oscilloscope screen, visually set $\alpha \approx 90°$ (i.e., the firing point is midway between the zero crossings of V_{ab}). Measure $V_{ab,rms}$ using both multimeter and oscilloscope. Record both $V_{ab,rms}$ readings, and α. Since the circuit is energized with $V_{an} = 70Vrms$, the value of $V_{ab,rms}$ for $\alpha \approx 90°$ should be approximately $\dfrac{70}{\sqrt{2}} =$ 49V. By comparing your oscilloscope and multimeter readings, can you tell if your multimeter reads true rms, or if it simply averages the rectified wave and makes a sinewave assumption?

Save screen snapshot #1

12. Set α to the maximum value that still has conduction. Use time cursors and determine α in degrees. Measure $V_{ab,rms}$, and record $V_{ab,rms}$ and α.

13. Turn the variac output voltage knob to zero, and then turn off the variac switch.
14. **Careful – when using two oscilloscope probes, remember the black alligator clips (i.e., "grounds") on these probes are connected together at the scope's BNC terminals.** Therefore, when using two probes, do not use the ground clip of the second probe. Instead, clip it onto itself so that it does not accidentally touch part of the dimmer circuit, establishing a short circuit through the BNC terminals. For example, connecting one probe across V_{ab}, and the other probe across V_{cn} will establish a short circuit from point b to point n.
15. Connect one oscilloscope probe to view variac output V_{an}, and a second probe to view capacitor voltage V_{cn}.

16. Re-energize your circuit with V_{an} = 70Vrms. Observe the variation of capacitor voltage V_{cn} (magnitude and phase with respect to variac output V_{an}) with α. In your report, comment on how your capacitor voltage observations compare with those in Excel program EE462L_Triac_Light_Dimmer.xls.

Diac conducts when V_{cn} reaches 32-35V (diac breakover voltage). The capacitor then discharges through the triac gate.

$\alpha = 90° \approx 16.67\text{ms} \div 4$
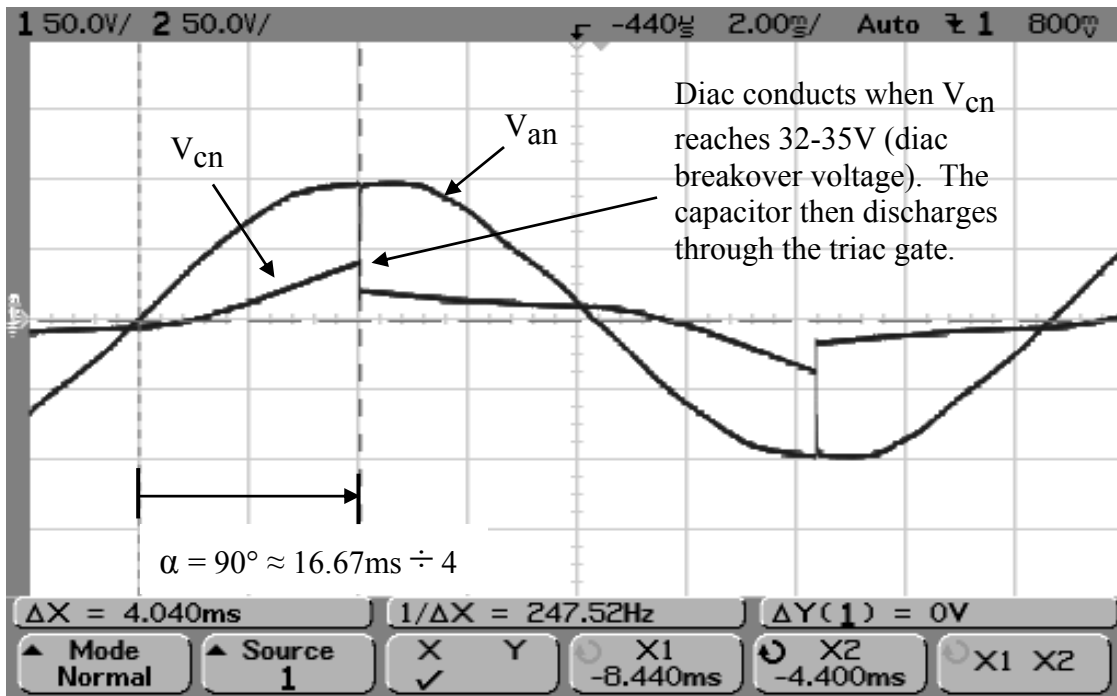
| ΔX = 4.040ms | 1/ΔX = 247.52Hz | ΔY(1) = 0V | Save screen snapshot #2 |

In the above screen snapshot, the time period corresponding to α is ΔX = 4.040ms

Source	Freq	Fixed R	Potentiometer kohm	C	Diac breakover	Diac on volts
Vrms	Hz	kohm		uF	V	V
70	60	3.3	49	0.1	35	5

EE362L_Triac_Light_Dimmer.xls
V_{an} and V_{cn} waveforms with potentiometer adjusted for $\alpha = 90°$

—— Source voltage —— Capacitor voltage —— Diac breakover
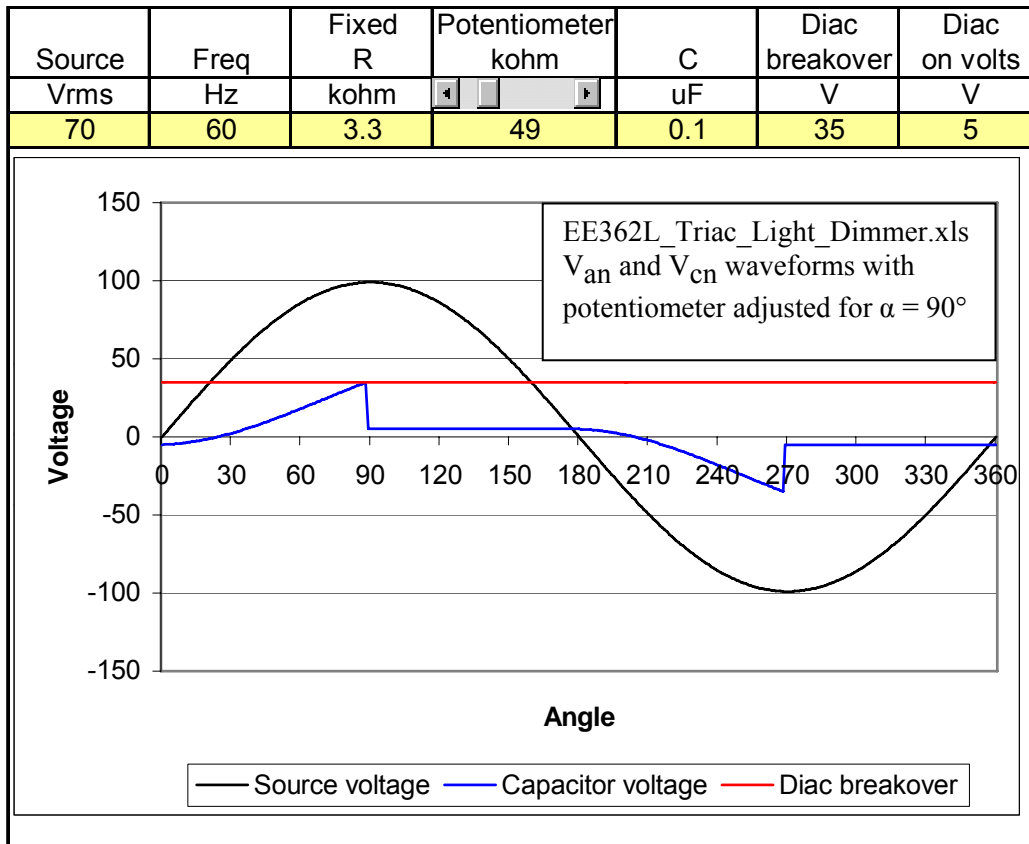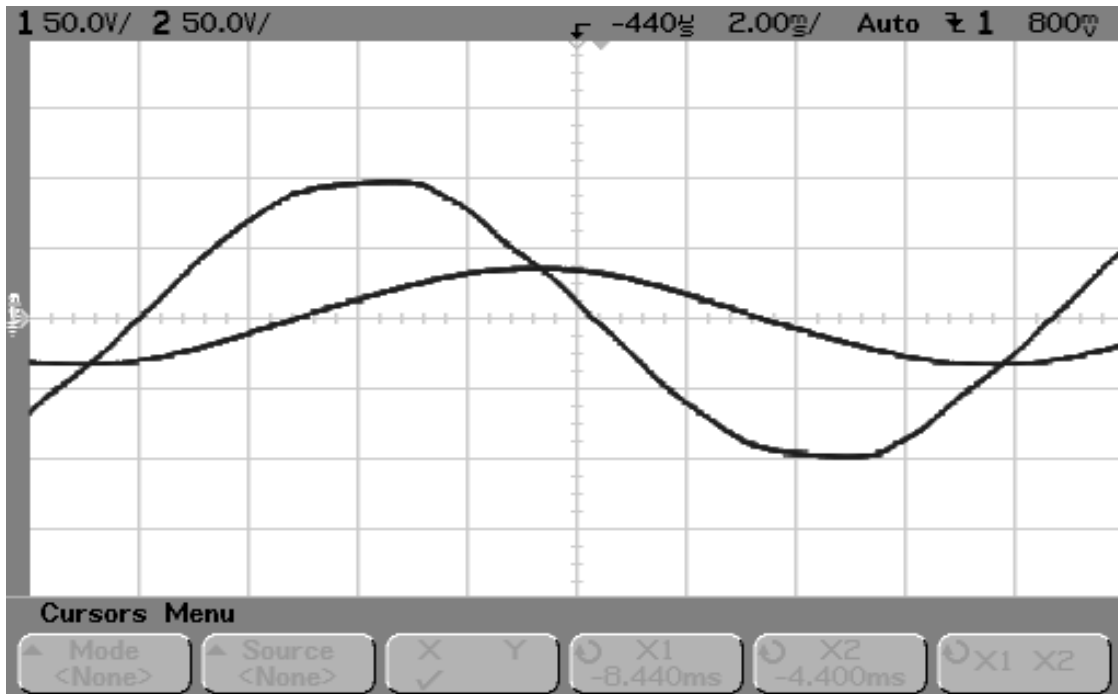
As potentiometer resistance increases, firing stops because V_{cn} never exceeds the diac breakover voltage. In that case, V_{cn} has a steady-state phasor solution. The above screen snapshot shows V_{an} and V_{cn} after transition into the no-firing regime.

Source	Freq	Fixed R	Potentiometer kohm	C	Diac breakover	Diac on volts
Vrms	Hz	kohm	◀ ▮ ▶	uF	V	V
70	60	3.3	96	0.1	35	5

EE462L_Triac_Light_Dimmer.xls waveforms after transition into the no-firing regime
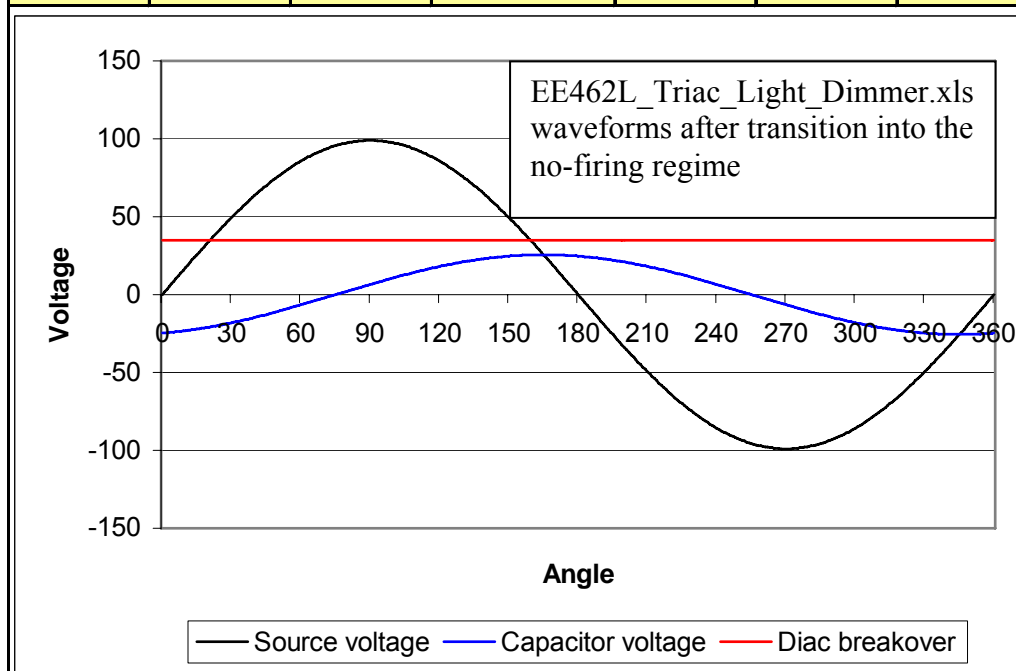
When there is no firing, the steady-state phasor solution for the capacitor voltage (ignoring the light bulb resistance) is

$$V_{cn} = V_{an}\left[\dfrac{\dfrac{1}{j\omega C}}{R + \dfrac{1}{j\omega C}}\right] = V_{an}\left[\dfrac{1}{1 + j\omega RC}\right],$$

where R is the series combination of the fixed and variable resistances. For small R, $V_{cn} \approx V_{an}$. As R increases, the $j\omega RC$ term begins to dominate, causing the magnitude of V_{cn} to decrease and lag V_{an}. As a result, values of α greater than 90° are possible.

E. Measure magnitudes of harmonic components of Vab

1. Using only one scope probe, with V_{an} = 70Vrms, view V_{ab} on the scope and set α ≈ 90°.
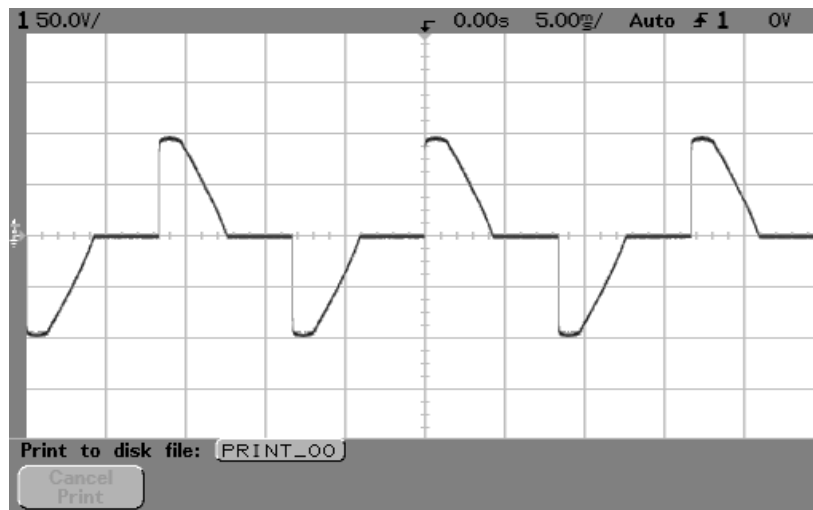
V_{ab} time trace, with Van ≈ 70Vrms, and α ≈ 90°

2. Set the horizontal scale so that at least three cycles of the waveform as shown.
3. Press the "Math" button, then "FFT," then "Settings."
4. Adjust "Span" to 1kHz, and "Center" to 500Hz.
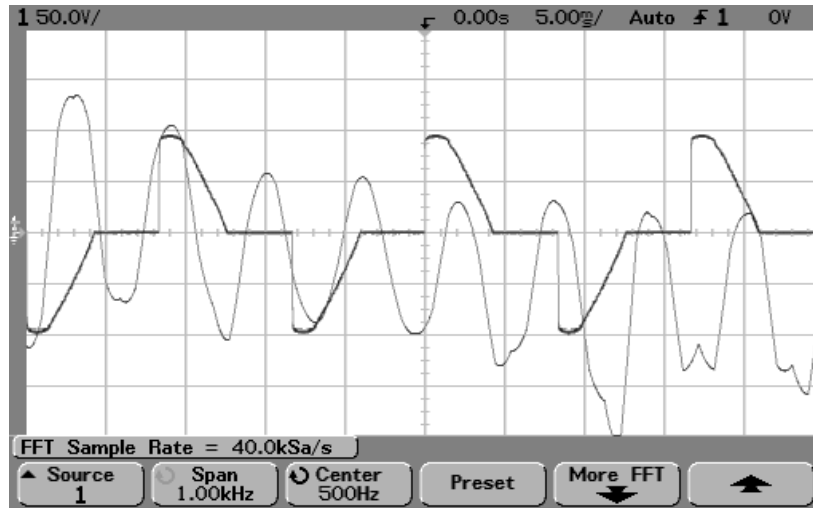
Spectral content of V_{ab}, superimposed on time trace (note –
spacing between vertical lines corresponds to 100Hz)

5.   Press "More FFT" to see the dB per division scale.
6.   Press "Math" to return.
7.   Press the "1" button to turn off the time trace.
8.   Press the "Cursors" button.
9.   Adjust Y1 to the top of the 60Hz component, and Y2 to the top of the 180Hz component.
10. Measure the dB values of the 60Hz and 180Hz components. These values are with respect to a 1Vrms reference.
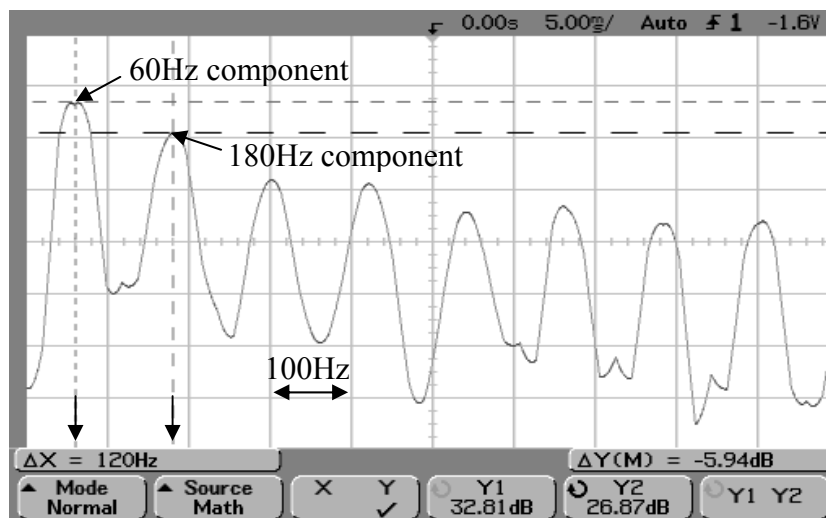
Measuring the dB difference between 60Hz and 180Hz
components of V_{ab}

11. Compute the ratio of V_{180}/V_{60} and compare the ratio to that predicted in Excel program EE462L_Triac_Light_Dimmer_Fourier_Waveform.xls.

Example calculations:

$$32.81db = 20\log_{10}\left(\frac{V_{60Hz}}{1Vrms}\right), \text{ so } V_{60Hz} = 1Vrms \bullet 10^{\left(\frac{32.81}{20}\right)} = 43.7Vrms$$

$$26.87db = 20\log_{10}\left(\frac{V_{180Hz}}{1Vrms}\right), \text{ so } V_{180Hz} = 1Vrms \bullet 10^{\left(\frac{26.87}{20}\right)} = 22.1Vrms$$

$$-5.94db = 20\log_{10}\left(\frac{V_{180Hz}}{V_{60Hz}}\right), \text{ so } \frac{V_{180Hz}}{V_{60Hz}} = 10^{\left(\frac{-5.94}{20}\right)} = 0.505.$$

F. 120Vac operation
Careful! Slowly raise the variac output voltage to 120Vrms, observe V_{ab} on the oscilloscope as you vary the firing angle from minimum to maximum, and verify that the circuit is working properly. The smooth operation should make it obvious that the circuit components have been optimized to work best at full 120Vrms input voltage. You may also be interested in powering up to 1kW of lights.

Lab report
Document your experiment, addressing the steps in parts C through E as needed. Many students include a digital photo of their circuit in their report. "Paste in" the requested screen snapshots. Use Excel, **with scatter plot option**, to plot your three oscilloscope-measured $V_{ab,rms}$ data points from Steps C10, C11, and C12 versus α in degrees, along with calculations using the theoretical formula below.

$$V_{ab,rms}^2 = V_{an,rms}^2\left[1 - \frac{\alpha}{\pi} + \frac{\sin 2\alpha}{2\pi}\right], \alpha \text{ in radians.} \tag{1}$$

Optional – using the definition of rms, can you derive the above theoretical formula?

Parts list
• Isolated case triac, 200V, 15A Littlefuse Q2015L5, (Mouser #576-Q2015L5)
• Heat sink for triac, approx. 1.5" x 1.75" for TO-220 case style, 9.6°C/W (Aavid Thermalloy, Mouser #532-507222B00)
• 32V trigger diode (diacs), STMicroelectronics DB3 or DB3TG, on-state voltage = 5V, (Mouser #511-DB3 or #511-DB3TG)
• 0.1μF, 100V axial lead ceramic capacitor (Kemet, Mouser #80-C430C104K1R) (in student parts bin)
• 250kΩ, ½W potentiometer with linear taper (Alpha/Xicon, Mouser #31VC503-F)
• 3.3kΩ, ¼W resistor (in student parts bin)

- One 3-terminal, 20A terminal block (Molex, Mouser #538-38780-0103). One of the center screws is removed and the hole marked with paint to indicate "don't use."
- 1" steel corner bracket for mounting the potentiometer (Stanley 30-3010, Home Depot). Hole in 1" bracket enlarged with 5/16" drill bit to fit the potentiometer.
- 1½" steel corner bracket for mounting the triac (Stanley 30-3170, Home Depot).
- 1" x 6" wood (approx. 10" long piece)
- Porcelain 120V light bulb holder
- 60W clear-glass bulb
- Two 9/16" or ½"outer diameter flat rubber water-faucet washers for the porcelain light bulb holder. A rubber washer goes between the screw head of the 1" screw and the porcelain to prevent the porcelain from cracking.
- A floppy diskette in anti-static bag. Each student should write his/her name on the floppy and use it all semester.
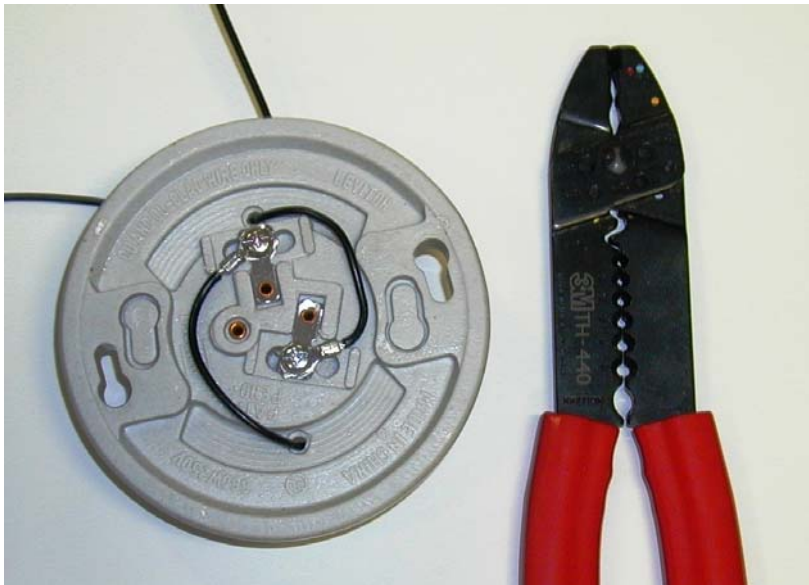
Extra parts for the student parts bin and screw cabinet, at least
- 5 of the triacs, and diacs
- 5 of the rubber washers

Plastic bags for parts
- 6"x8", 6mil for light bulb
- 6"x8", 6mil for porcelain socket
- 4"x6", 4mil antistatic for small parts
- 8"x10", 6mil for holding everything

#6-32, ½" machine screw,
flat washer, split washer, and
hex nut

Flat rubber washers between
#8 x 1" screws and porcelain

Remove this center screw

#8 x ½" screws for corner brackets

#8 x 3/4" screws for terminal blocks

Remove this center screw

The back of the triac fits
firmly against the heat sink,
with maximum surface
contact. The flat washer,
then split washer, then hex
nut fit on the other side of the
corner bracket.
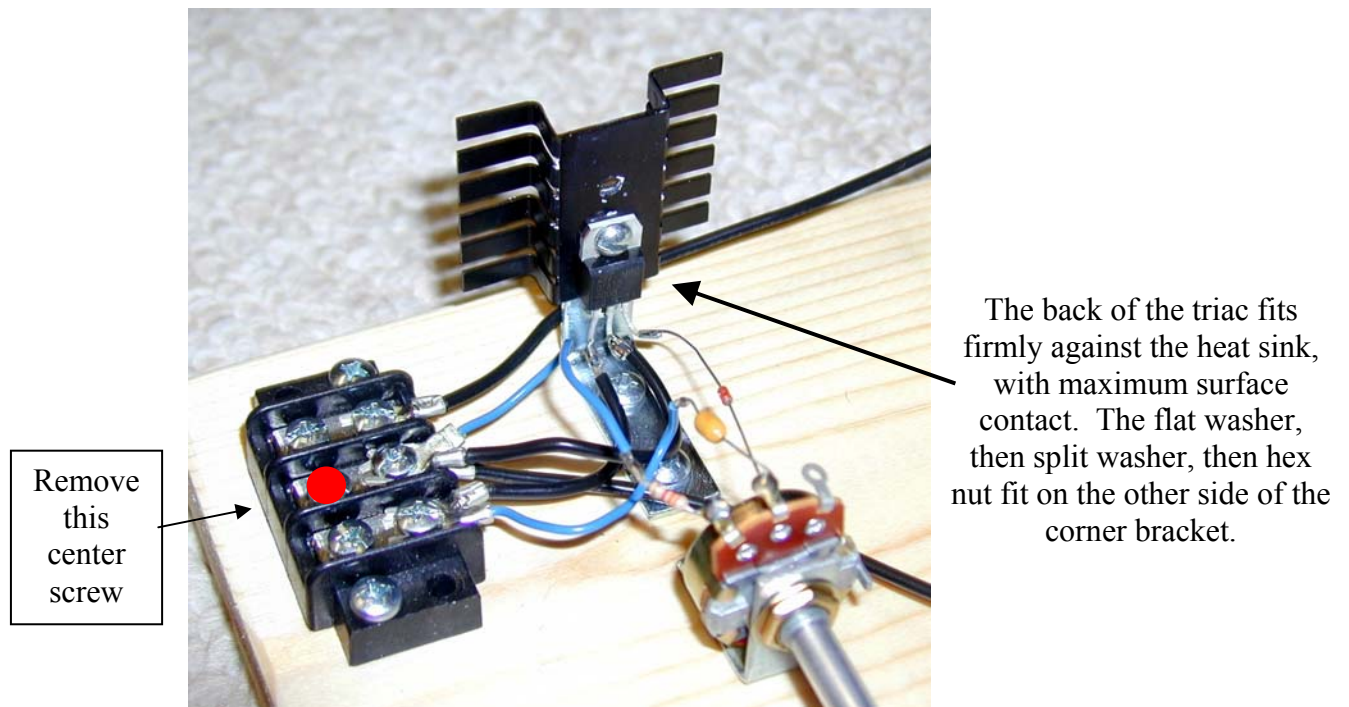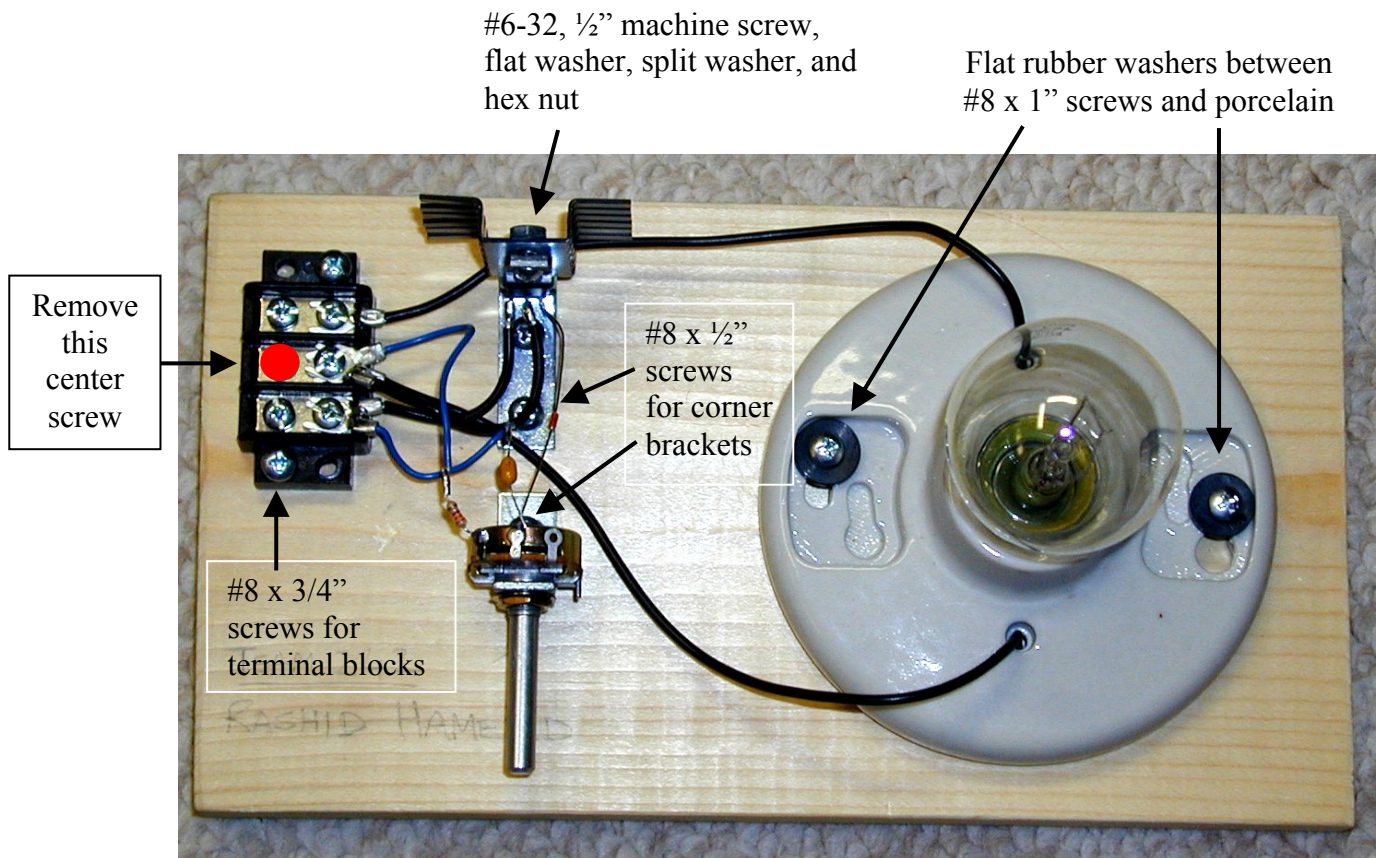
Appendix

RMS
The rms value of a periodic current (or voltage) waveform is defined as

$$I_{rms} = \sqrt{I_{rms}^2} \text{ , where } I_{rms}^2 = \frac{1}{T}\int_{t}^{t+T} i^2(t)dt \text{ .}$$

Evaluating the integral for the special case of a sine wave of current shows that the rms value is the peak current divided by $\sqrt{2}$.

Fourier Series
Any physically realizable periodic waveform can be decomposed into a Fourier series of average (i.e., DC), fundamental frequency, and harmonic terms. In sine form, the Fourier series in polar form is

$$i(t) = I_{avg} + \sum_{k=1}^{\infty} I_k \sin(k\omega_o t + \theta_k) = I_{avg} + \sum_{k=1}^{\infty} I_k \cos(k\omega_o t + \theta_k - 90^o) \text{ ,}$$

where I_{avg} is the average value, I_k are peak magnitudes of the individual harmonics, ω_o is the fundamental frequency (in radians per second), and θ_k are the harmonic phase angles. The time period of the waveform is

$$T = \frac{2\pi}{\omega_o} = \frac{2\pi}{2\pi f_o} = \frac{1}{f_o} \text{ .}$$

The formulas for computing I_{avg} , I_k , θ_k are well known and can be found in any undergraduate electrical engineering textbook on circuit analysis. These are described in a following section.

Figure A.1 shows a desktop computer (i.e., PC) current waveform. The figure illustrates how the actual waveform can be approximated by summing only the fundamental, 3rd, and 5th harmonic components. If higher-order terms are included (i.e., 7th, 9th, 11th, and so on), then the original PC current waveform will be perfectly reconstructed. A truncated Fourier series is actually a least-squared error curve fit. As higher frequency terms are added, the error is reduced.

Fortunately, a special property known as half-wave symmetry exists for most power electronic loads. Have-wave symmetry exists when the positive and negative halves of a waveform are identical but opposite, i.e.,

$$i(t) = -i(t \pm \frac{T}{2}) \text{ ,}$$

where *T* is the period. Waveforms with half-wave symmetry have no even-ordered harmonics.
It is obvious that the PC current waveform is half-wave symmetric. Televisions and other home
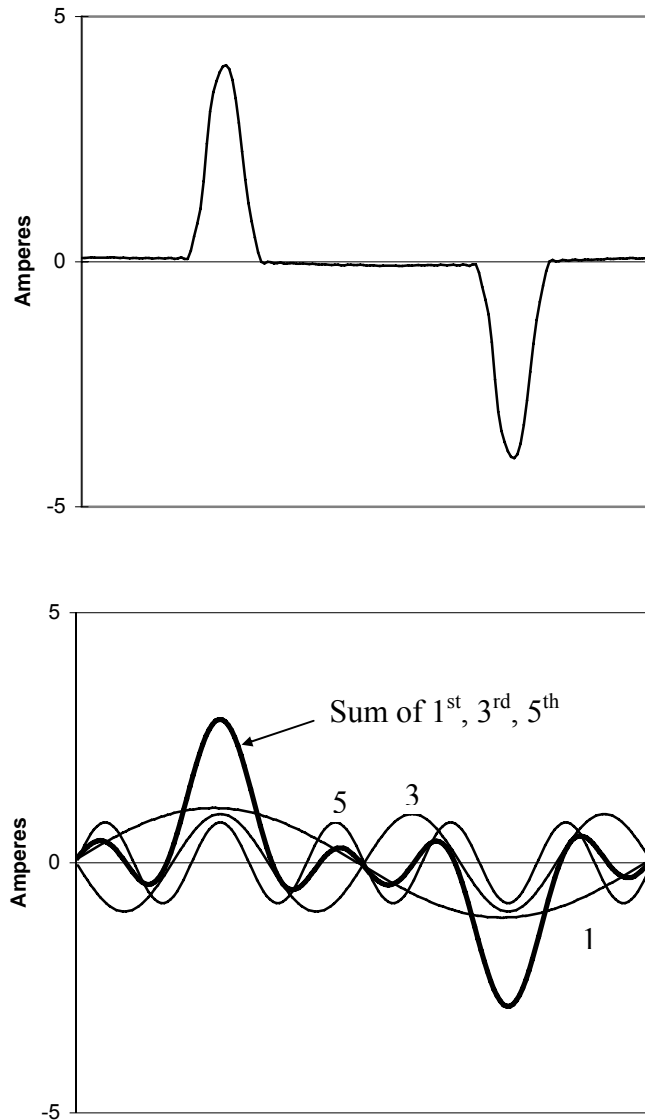entertainment equipment have the same waveform.

Figure A.1. PC Current Waveform, and its 1st, 3rd, and 5th Harmonic Components

Fourier Coefficients

If function $i(t)$ is periodic with an identifiable period T (i.e., $i(t) = i(t \pm NT)$), then $i(t)$ can be written in rectangular form as

$$i(t) = I_{avg} + \sum_{k=1}^{\infty} \left[a_k \cos(k\omega_o t) + b_k \sin(k\omega_o t) \right], \ \omega_o = \frac{2\pi}{T},$$

where

$$I_{avg} = \frac{1}{T} \int_{t_o}^{t_o + T} i(t) dt,$$

$$a_k = \frac{2}{T} \int_0^T i(t) \cos(k\omega_o t) dt,$$

$$b_k = \frac{2}{T} \int_0^T i(t) \sin(k\omega_o t) dt.$$

The sine and cosine terms above can be converted to the convenient polar form by using trigonometry as follows:

$$a_k \cos(k\omega_o t) + b_k \sin(k\omega_o t)$$

$$= \sqrt{a_k^2 + b_k^2} \bullet \frac{a_k \cos(k\omega_o t) + b_k \sin(k\omega_o t)}{\sqrt{a_k^2 + b_k^2}}$$

$$= \sqrt{a_k^2 + b_k^2} \bullet \left[\frac{a_k}{\sqrt{a_k^2 + b_k^2}} \cos(k\omega_o t) + \frac{b_k}{\sqrt{a_k^2 + b_k^2}} \sin(k\omega_o t) \right]$$

$$= \sqrt{a_k^2 + b_k^2} \bullet \left[\sin(\theta_k) \cos(k\omega_o t) + \cos(\theta_k) \sin(k\omega_o t) \right],$$

where

$$\sin(\theta_k) = \frac{a_k}{\sqrt{a_k^2 + b_k^2}}, \ \cos(\theta_k) = \frac{b_k}{\sqrt{a_k^2 + b_k^2}}.$$

Applying trigonometric identity

$$\sin(A + B) = \sin(A) \cos(B) + \cos(A) \sin(B),$$
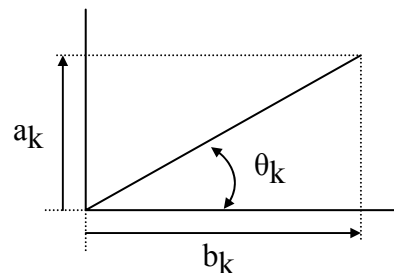
yields polar form

$$\sqrt{a_k^2 + b_k^2} \bullet \sin(k\omega_o t + \theta_k),$$

where

$$\tan(\theta_k) = \frac{\sin(\theta_k)}{\cos(\theta_k)} = \frac{a_k}{b_k}.$$

Phase Shift
If the PC waveform in Figure A.2 is delayed by ΔT seconds, the modified current is
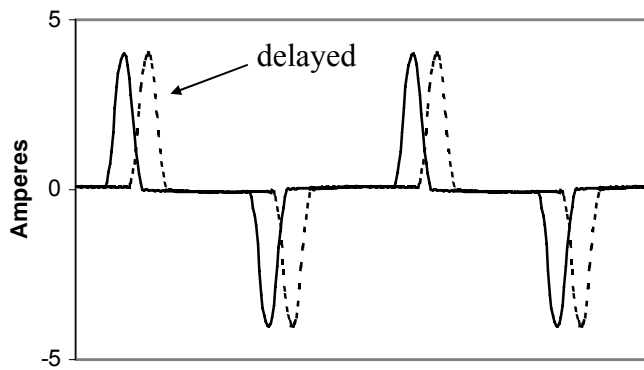
Figure A.2. PC Current Waveform Delayed in Time

$$i(t - \Delta T) = \sum_{k=1}^{\infty} I_k \sin(k\omega_o(t - \Delta T) + \theta_k) = \sum_{k=1}^{\infty} I_k \sin(k\omega_o t - k\omega_o \Delta T + \theta_k)$$

$$= \sum_{k=1}^{\infty} I_k \sin(k\omega_o t + (\theta_k - k\omega_o \Delta T)) = \sum_{k=1}^{\infty} I_k \sin(k\omega_o t + \theta_k - k\theta_o),$$

where θ_o is the phase lag of the fundamental current corresponding to ΔT. The last term above shows that individual harmonics are delayed by $k\theta_o$ of their own degrees.

Symmetry Simplifications
Waveform symmetry greatly simplifies the effort in developing Fourier coefficients. Symmetry arguments should be applied to the waveform **after the average value has been removed**. The most important cases are

    Odd Symmetry, i.e., $i(t) = -i(-t)$,

        then the corresponding Fourier series has **no cosine terms**,

$$a_k = 0 ,$$

and b_k can be found by integrating over the **first half-period** and **doubling** the results,

$$b_k = \frac{4}{T} \int_0^{T/2} i(t) \sin(k\omega_o t) dt .$$

Even Symmetry, i.e., $i(t) = i(-t)$,

then the corresponding Fourier series has **no sine terms**,

$$b_k = 0 ,$$

and a_k can be found by integrating over the **first half-period** and **doubling** the results,

$$a_k = \frac{4}{T} \int_0^{T/2} i(t) \cos(k\omega_o t) dt .$$

Important note – even and odd symmetry can sometimes be obtained by time-shifting the waveform. In this case, solve for the Fourier coefficients using the time-shifted waveform, and then phase-shift the Fourier coefficient angles according to (A.6).

Half-Wave Symmetry, i.e., $i(t \pm \frac{T}{2}) = -i(t)$,

then the corresponding Fourier series has **no even harmonics**, and a_k and b_k can be found by integrating over **any half-period** and **doubling** the results,

$$a_k = \frac{4}{T} \int_{t_o}^{t_o + T/2} i(t) \cos(k\omega_o t) dt , \quad k \text{ odd},$$

$$b_k = \frac{4}{T} \int_{t_o}^{t_o + T/2} i(t) \sin(k\omega_o t) dt , \quad k \text{ odd}.$$

Half-wave symmetry is common in power systems.

Examples

Square Wave

By inspection, the average value is zero, and the waveform has both odd symmetry and half-wave symmetry. Thus, $a_k = 0$, and

$$b_k = \frac{4}{T}\int_{t_o}^{t_o+T/2} v(t)\sin(k\omega_o t)dt, \ k \ \text{odd}.$$
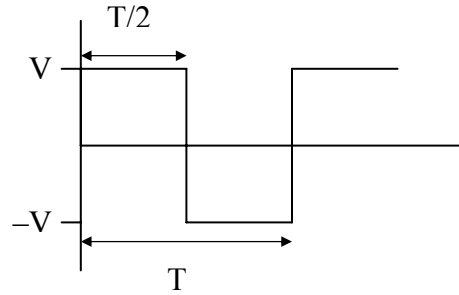
Solving for b_k,

$$b_k = \frac{4}{T}\int_0^{T/2} V\sin(k\omega_o t)dt = \frac{-4V}{k\omega_o T}\cos(k\omega_o t)\Big|_{t=0}^{t=T/2} = \frac{-4V}{k\omega_o T}\left(\cos\left(\frac{k\omega_o T}{2}\right) - \cos(0)\right)$$

Since $\omega_o = \frac{2\pi}{T}$, then

$$b_k = \frac{-4V}{2k\pi}\left(\cos(k\pi) - 1\right) = \frac{2V}{k\pi}\left(1 - \cos(k\pi)\right), \text{ yielding}$$

$$b_k = \frac{4V}{k\pi}, \ k \ \text{odd}.$$

The Fourier series is then

$$v(t) = \frac{4V}{\pi}\sum_{k=1, \, k \, odd}^{\infty}\frac{1}{k}\sin(k\omega_o t) = \frac{4V}{\pi}\left[\sin(1\omega_o t) + \frac{1}{3}\sin(3\omega_o t) + \frac{1}{5}\sin(5\omega_o t) + \cdots\right].$$

Note that the **harmonic magnitudes decrease according to** $\frac{1}{k}$.

Triangle Wave

By inspection, the average value is zero, and the waveform has both even symmetry and half-wave symmetry. Thus, $b_k = 0$, and

$$a_k = \frac{4}{T}\int_{t_o}^{t_o+T/2} v(t)\cos(k\omega_o t)dt, \ k \ \text{odd}.$$
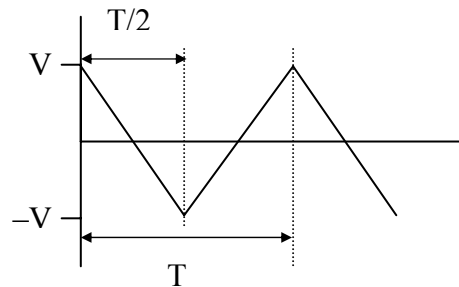
Solving for a_k,

$$a_k = \frac{4}{T}\int_0^{T/2} V\left(1-\frac{4t}{T}\right)\cos(k\omega_o t)dt = \frac{4V}{T}\int_0^{T/2}\cos(k\omega_o t)dt - \frac{16V}{T^2}\int_0^{T/2} t\cos(k\omega_o t)dt$$

$$= \frac{4V}{k\omega_o T}\left(\sin\left(\frac{k\omega_o T}{2}\right)-\sin(0)\right) - \frac{16V}{T^2}\frac{t\sin(k\omega_o t)}{k\omega_o}\bigg|_{t=0}^{t=T/2} + \frac{16V}{T^2}\int_0^{T/2}\frac{\sin(k\omega_o t)}{k\omega_o}dt$$

$$\frac{2V}{k\pi}\sin(k\pi)-\frac{4V}{k\pi}\sin(k\pi)+\frac{4V}{k^2\pi^2}(1-\cos(k\pi)),\ k\ \text{odd.}$$

Continuing,

$$a_k = \frac{8V}{k^2\pi^2}\ ,\ k\ \text{odd}$$

The Fourier series is then

$$v(t) = \frac{8V}{\pi^2}\sum_{k=1,\,k\ odd}^{\infty}\frac{1}{k^2}\cos(k\omega_o t)$$

$$= \frac{8V}{\pi^2}\left[\cos(1\omega_o t)+\frac{1}{9}\cos(3\omega_o t)+\frac{1}{25}\cos(5\omega_o t)+\cdots\right],$$

where it is seen that the **harmonic magnitudes decrease according to** $\frac{1}{k^2}$.

To convert to a sine series, recall that $\cos(\theta)=\sin(\theta+90^o)$, so that the series becomes

$$v(t) = \frac{8V}{\pi^2}\left[\sin(1\omega_o t+90^o)+\frac{1}{9}\sin(3\omega_o t+90^o)+\frac{1}{25}\sin(5\omega_o t+90^o)+\cdots\right].$$

To time delay (i.e., move to the right) the waveform by $\frac{T}{4}$ (i.e., 90° of fundamental),
subtract $(k\bullet 90^o)$ from each harmonic angle. Then, the above series becomes

$$v(t) = \frac{8V}{\pi^2}\left[\sin(1\omega_o t+90^o-1\bullet 90^o)+\frac{1}{9}\sin(3\omega_o t+90^o-3\bullet 90^o)\right.$$
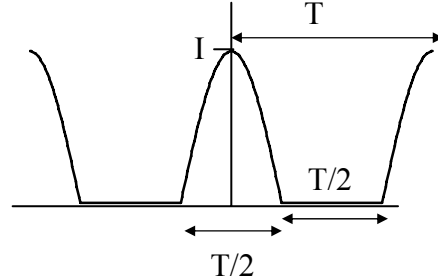$$\left.+\frac{1}{25}\sin(5\omega_o t+90^o-5\bullet 90^o)+\cdots\right],$$

or

$$v(t) = \frac{8V}{\pi^2}\left[\sin(1\omega_o t) - \frac{1}{9}\sin(3\omega_o t) + \frac{1}{25}\sin(5\omega_o t) - \frac{1}{49}\sin(7\omega_o t)\cdots \right].$$

Half-Wave Rectified Cosine Wave

The waveform has an average value and even symmetry. Thus, $b_k = 0$, and

$$a_k = \frac{4}{T}\int_0^{T/2} i(t)\cos(k\omega_o t)dt, \ k \text{ odd.}$$

Solving for the average value,

$$I_{avg} = \frac{1}{T}\int_{t_o}^{t_o+T} i(t)dt = \frac{1}{T}\int_{-T/4}^{T/4} I\cos(\omega_o t)dt = \frac{I}{\omega_o T}\sin(\omega_o t)\Big|_{t=-T/4}^{t=T/4}$$

$$= \frac{I}{2\pi}\left(\sin\frac{\omega_o T}{4} - \sin\frac{-\omega_o T}{4}\right) = \frac{I}{\pi}\sin\frac{\omega_o T}{4} = \frac{1}{\pi}\sin\frac{\pi}{2}.$$

$$I_{avg} = \frac{I}{\pi}.$$

Solving for a_k,

$$a_k = \frac{4}{T}\int_0^{T/4} I\cos(\omega_o t)\cos(k\omega_o t)dt = \frac{2I}{T}\int_0^{T/4}(\cos(1-k)\omega_o t + \cos(1+k)\omega_o t)dt$$

$$= \frac{2I}{T}\left(\frac{\sin(1-k)\omega_o t}{(1-k)\omega_o} + \frac{\sin(1+k)\omega_o t}{(1+k)\omega_o}\right)\Big|_{t=0}^{t=T/4}.$$

For $k = 1$, taking the limits of the above expression when needed yields

$$a_1 = \frac{2I}{T} \bullet \lim_{(1-k)\omega_o \to 0}\left(\frac{\sin(1-k)\omega_o \frac{T}{4}}{(1-k)\omega_o}\right) + \frac{I}{\pi}\frac{\sin(1+1)\frac{\pi}{2}}{(1+1)\omega_o}$$

$$- \frac{2I}{T} \bullet \lim_{(1-k)\omega_o \to 0}\frac{\sin(1-k)\omega_o \bullet 0}{(1-k)\omega_o} - \frac{I}{\pi}\frac{\sin(0)}{(1+1)\omega_o}$$

$$a_1 = \frac{2I}{T}\frac{T}{4} + \frac{I}{2\omega_o\pi}\sin(\pi) - 0 - 0 = \frac{I}{2}.$$

For $k > 1$,

$$a_k = \frac{I}{\pi}\left(\frac{\sin(1-k)\frac{\pi}{2}}{(1-k)} + \frac{\sin(1+k)\frac{\pi}{2}}{(1+k)}\right).$$

All odd k terms above are zero. For the even terms, it is helpful to find a common denominator and express the above equation as

$$a_k = \frac{I}{\pi}\left(\frac{(1+k)\sin(1-k)\frac{\pi}{2} + (1-k)\sin(1+k)\frac{\pi}{2}}{1-k^2}\right), \quad k > 1,\ k \text{ even.}$$

Evaluating the above equation shows an alternating sign pattern that can be expressed as

$$a_k = \frac{2I}{\pi}\sum_{k=2,4,6,\cdots}^{\infty}(-1)^{\frac{k+2}{2}}\frac{1}{k^2-1}, \quad k > 1,\ k \text{ even.}$$

The final expression becomes

$$i(t) = \frac{I}{\pi} + \frac{I}{2}\cos(\omega_o t) + \frac{2I}{\pi}\sum_{k=2,4,6,\cdots}^{\infty}(-1)^{k/2+1}\frac{1}{k^2-1}\cos(k\omega_o t)$$

$$= \frac{I}{\pi} + \frac{I}{2}\cos(\omega_o t) + \frac{2I}{\pi}\left[\frac{1}{3}\cos(2\omega_o t) - \frac{1}{15}\cos(4\omega_o t) + \frac{1}{35}\cos(6\omega_o t) - \cdots\right].$$

Light Dimmer Current
The Fourier coefficients of the waveform in Figure 1 can be shown to be the following:

For the fundamental,

$$a_1 = \frac{-V_p}{\pi}\sin^2\alpha, \quad b_1 = V_p\left[1 - \frac{\alpha}{\pi} + \frac{1}{2\pi}\sin 2\alpha\right],$$

where V_p is the peak value of the underlying AC waveform, and α is in radians.

For harmonic multiples above the fundamental (i.e., $k = 3, 5, 7, \ldots$),

$$a_k = \frac{V_p}{\pi}\left[\frac{1}{1-k}\big(\cos(1-k)\alpha - \cos(1-k)\pi\big) + \frac{1}{1+k}\big(\cos(1+k)\alpha - \cos(1+k)\pi\big)\right],$$

$$b_k = \frac{V_p}{\pi}\left[\frac{1}{1-k}\big(\sin(1-k)\pi - \sin(1-k)\alpha\big) + \frac{1}{1+k}\big(\sin(1+k)\alpha - \sin(1+k)\pi\big)\right].$$

The waveform has zero average, and it has no even harmonics because of half-wave symmetry.

The magnitude of any harmonic k, including $k = 1$, is $V_k = \sqrt{a_k^2 + b_k^2}$. Performing the calculations with $\alpha = \dfrac{\pi}{2}$ radians (i.e., 90°) yields

$$V_1 = \frac{V_p}{\pi}\sqrt{1 + \frac{\pi^2}{4}} = 0.593\,V_p, \text{ and } V_3 = \frac{V_p}{\pi} = 0.318\,V_p,$$

so that

$$\frac{V_3}{V_1} = \frac{1}{\sqrt{1 + \dfrac{\pi^2}{4}}} = 0.537.$$

The above case is illustrated in the following Excel spreadsheet.

Excel Program EE462L_Triac_Light_Dimmer_Fourier_Waveform.xls

Triac_Light_Dimmer_Fourier_Waveform.xls. Light Dimmer Voltage Waveform (normalized to peak value of underlying sine wave)

Enter
Alpha = 90   1.570796

k	Fourier ak	Fourier bk	Magk	Ratio Magk/Mag1
1	-0.31831	0.5	0.592724	1.000
3	0.31831	-3.9E-17	0.31831	0.537
5	-0.106103	3.9E-17	0.106103	0.179
7	0.106103	-3.9E-17	0.106103	0.179
9	-0.063662	3.9E-17	0.063662	0.107
11	0.063662	-3.9E-17	0.063662	0.107
13	-0.045473	3.9E-17	0.045473	0.077
15	0.045473	-3.9E-17	0.045473	0.077
17	-0.035368	3.9E-17	0.035368	0.060
19	0.035368	-3.9E-17	0.035368	0.060
21	-0.028937	1.93E-16	0.028937	0.049
23	0.028937	-1.93E-16	0.028937	0.049
25	-0.024485	-9.15E-17	0.024485	0.041
27	0.024485	9.15E-17	0.024485	0.041
29	-0.021221	1.52E-16	0.021221	0.036
31	0.021221	-1.52E-16	0.021221	0.036
33	-0.018724	-6.08E-17	0.018724	0.032
35	0.018724	6.08E-17	0.018724	0.032
37	-0.016753	1.28E-16	0.016753	0.028
39	0.016753	-1.28E-16	0.016753	0.028
41	-0.015158	-4.18E-17	0.015158	0.026
43	0.015158	9.32E-17	0.015158	0.026
45	-0.01384	6.13E-17	0.01384	0.023
47	0.01384	-1.13E-16	0.01384	0.023
49	-0.012732	-2.89E-17	0.012732	0.021

Light Dimmer Voltage Waveform

Note – the magnitude of the fundamental is computed to be 0.593 times the magnitude of the underlying sine wave (see Magk column). If the underlying sine wave is 70Vrms, this corresponds to 41.5Vrms, which is close to the Section D calculation. The ratio of the 3rd harmonic voltage magnitude to the fundamental is computed to be 0.537, which also compares favorably with Section D. Differences are most likely the fact that the wall outlet voltage is not an ideal sine wave, and also to errors in measuring α.

Triac Light Dimmer Modified to Serve as a Voltage Clamp

This circuit helps prevent voltage runaway on the output of a DC-DC boost or buck/boost converter. When the voltage across the diac reaches its 35V trigger level, the triac and 150W light bulb turn on, thus loading down the converter significantly, which helps to limit the converter's output voltage.
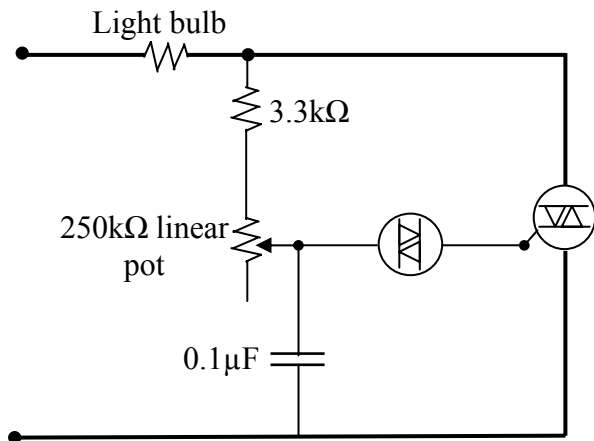
Original Triac Light Dimmer Circuit
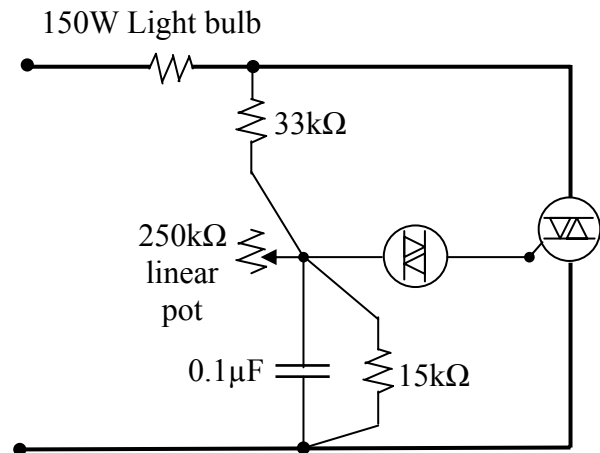
Modified Circuit that Turns On at Approximately 120V

Steps:

- Remove the 3.3kΩ resistor, and replace it with a 33kΩ, ½W resistor (in student parts bin). Solder the 33kΩ resistor to the diac/capacitor terminal of the 250kΩ potentiometer
- Solder a 15kΩ resistor (in student parts bin) across the 0.1μF capacitor
- Replace the 60W light bulb with a 150W light bulb

Note: After completing the above steps, the potentiometer of the original triac light dimmer is effectively disabled, but it is still useful as a soldering terminal.

EE462L, Power Electronics, Capacitor Filtered Diode Bridge Rectifier
Version Sept. 8, 2010

Overview
Electronic loads, such as desktop computers and televisions, operate on DC rather than AC. However, power is distributed in the U.S. through a 60Hz AC system. Electronic loads have a capacitor filtered, diode bridge rectifier that converts the incoming AC to DC. Later, we will learn how to efficiently reduce rectifier V_{dc} outputs to more useable values such as $12V_{dc}$.

This is a two-week team project, and the rectifier circuit that you and your partner build will be used many times during this semester and in future semesters. Combined with the $25V_{ac}$ transformer source, it will produce approximately the same $36\text{-}40V_{dc}$ that solar panel pairs on the ENS roof produce. **So, please build a neat, rugged circuit that will last, and solder your connections properly!** When finished, neatly print your team member names on the wood with a dark pen or permanent marker **for all to see clearly**.

Important
Do not energize your circuit until it has been inspected by Dr. Grady or one of the TAs. Carefully check the polarity of the diode bridge and capacitor carefully – **electrolytic capacitors can explode if they are reverse biased**. You will connect $28V_{ac}$ to your DBR.

Basics of Circuit Operation
The basic components of the single-phase rectifier are four diodes and a large electrolytic capacitor. The four diodes are often packaged together as one four-terminal device. The diodes rectify the incoming V_{ac}, and the capacitor smoothes the peak-to-peak ripple voltage in V_{dc} to a reasonable value (e.g., 5-10% of peak V_{dc}).

The basic rectifier circuit is shown below in Figure 1. When V_{ac} is positive, diodes 1 and 2 conduct, while diodes 3 and 4 are reverse-biased and open. When V_{ac} is negative, diodes 3 and 4 conduct, while diodes 1 and 2 are reverse-biased and open.
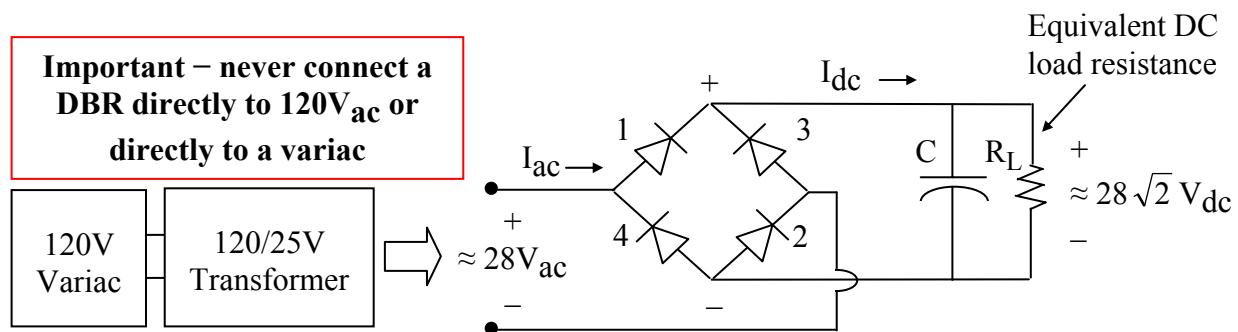
Figure 1. Single-Phase Diode Bridge with Capacitor Filter

Important note on safety: There are two hazards if you connect a variac directly to a DBR. First, and most important, is because when using a variac it is very easy to accidentally apply more than $35V_{ac}$ to the DBR, which when rectified exceeds the 50V rating of the capacitor. If you accidentally apply $120V_{ac}$, then the capacitor voltage can reach 165V! The capacitor can rupture or explode when severely overvoltaged, and the circuit breaker inside the variac may not prevent this from happening.

Second, the variac does not isolate the power ground from the load. Thus, when you touch the variac "hot" output, you can get a shock. But if you use a dual-winding transformer, like the 120/25 transformers in the lab, then the output has no ground reference. With no ground reference, you can still get shocked, but you must contact both terminals of the transformer output for this to happen.

To better understand the operation of the circuit, imagine that the capacitor is removed. Diodes 1 and 2 conduct when $V_{ac} > 0$. Diodes 3 and 4 conduct when $V_{ac} < 0$. The resulting voltage waveforms with $V_{ac} = 28V$ are shown in Figure 2.
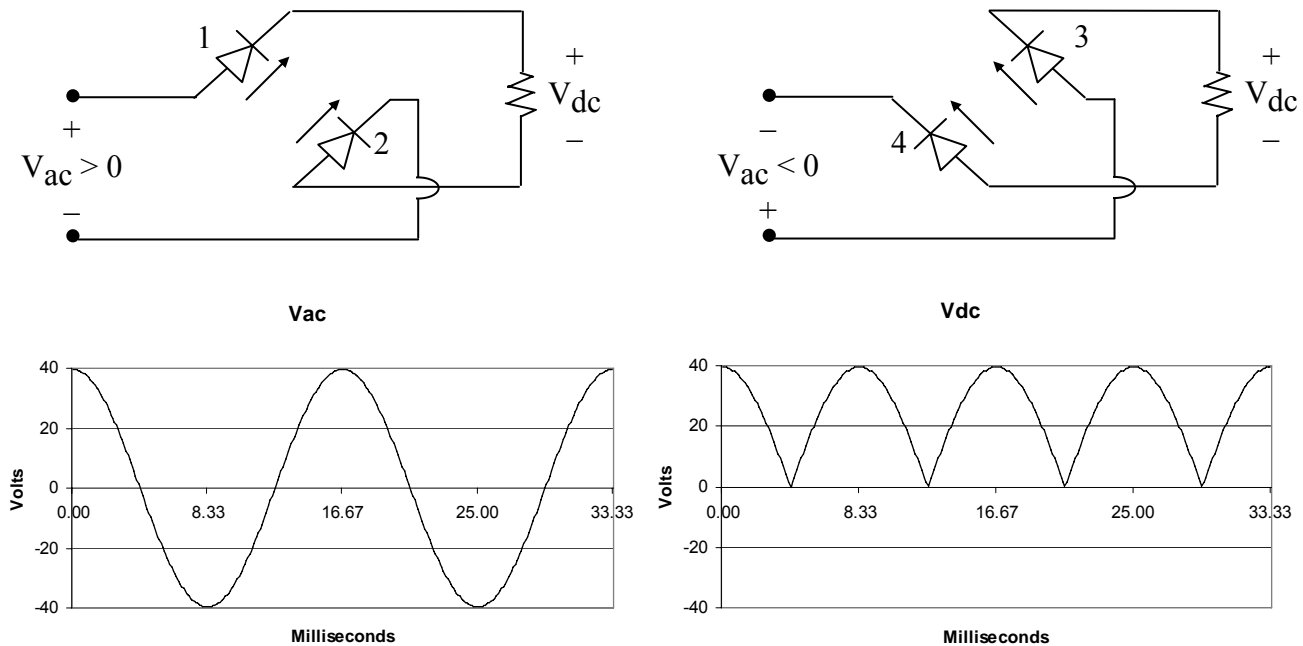
Figure 2. AC and DC Voltage Waveforms with a DC Load Resistor and No Capacitor

The addition of capacitor C smoothes the DC voltage waveform. If time constant R_LC significantly exceeds $\dfrac{T}{2}$, where $T = \dfrac{1}{f}$, then the capacitor provides load power when the rectified AC voltage falls below the capacitor voltage. As simulated by Excel program EE362L_Diode_Bridge_Rectifier.xls for the case shown below,

F - Hz	C - uF	VAC	P - W
60	18000	28	200

,

the waveform for V_{dc} takes the form of V_{cap} in Figure 3.
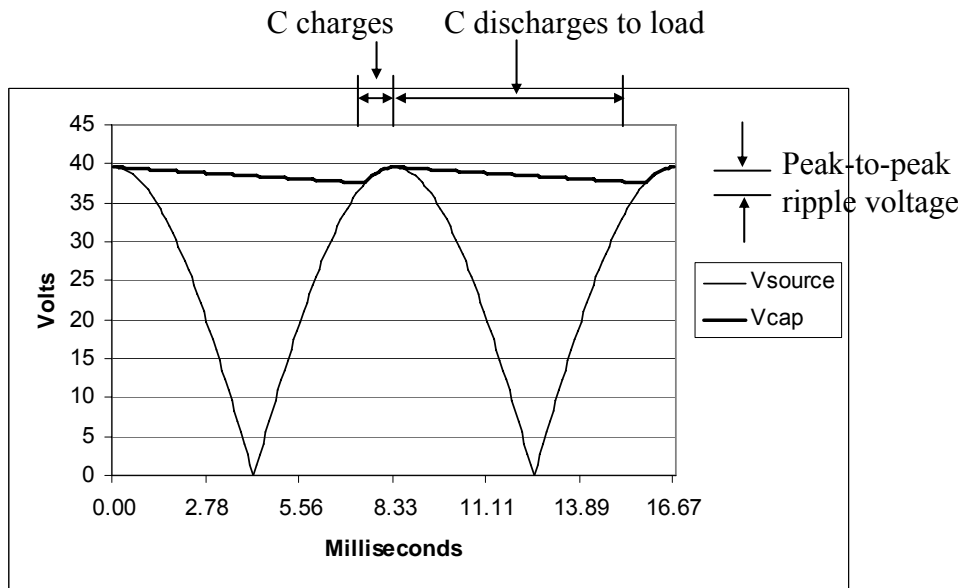
Figure 3. Impact of C on Load Voltage

As the load power increases, the capacitor discharges faster, the peak-to-peak ripple voltage increases, and the average dc voltage (i.e., the average value of the V_{cap} curve in Figure 3) falls. For zero load, V_{cap} remains equal to the peak of the rectified source voltage, and the ripple voltage is therefore zero.

Current and power flow from the AC side only when C is charging. When not charging, the voltage on C is greater than the rectified source voltage, and the diodes prevent current from flowing back into the AC side. Thus, AC current and power flow into the circuit in relatively short "bursts." As load power increases, the width of the current bursts becomes wider and taller, as illustrated in Figure 4. The precise shape of the current pulse depends on system impedance. If the impedance is mainly resistive, the current pulses resemble the top portions of sine waves. Inductance in the system impedance causes a skewing to the right.

200W Load   800W Load   *See note below
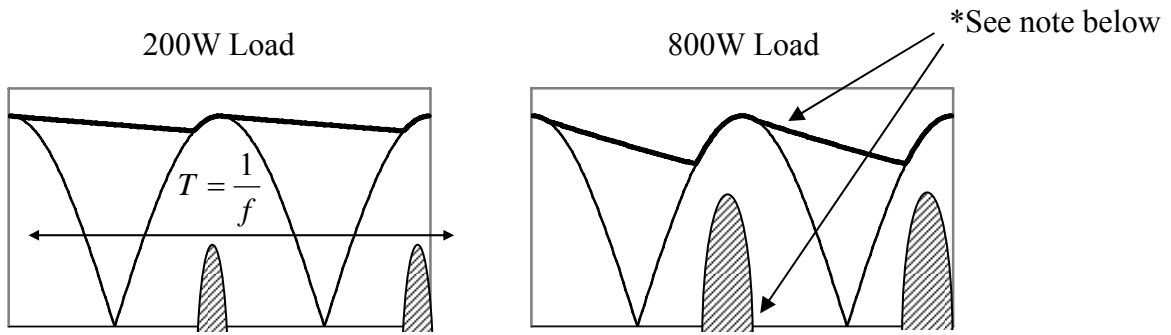
Figure 4. DC-Side Current i_{dc} for Two Different Load Levels
(This figure shows how the average voltage to the load drops as load power increases.
This phenomenon is due to the capacitor action and is not due to DBR resistance.)

* Inductance in the power system and transformer will cause the current to flow after the peak of the voltage curve. In that case, the capacitor voltage will follow the rectified voltage wave for some time after the peak. The higher the power level, the longer the current flows.

Reflected to the AC-side, the current is alternating with zero average value and half-wave symmetry, as shown below in Figure 5 for the 200W example.
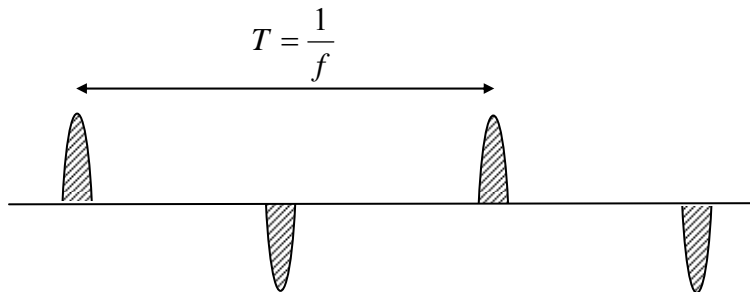
Figure 5. AC-Side Current I_{ac}

Estimation of DC Ripple Voltage for Constant Power Loads
Most power electronic loads require constant power. Thus, representing the load as a fixed resistor, as shown in Figure 1, is not exactly correct.

For constant power cases, peak-to-peak voltage ripple can be computed using energy balance in the capacitor as follows. If the "C discharging" period in Figure 3 is Δt, where $\dfrac{T}{4} \le \Delta t \le \dfrac{T}{2}$, then the energy provided by C during Δt is

$$\frac{1}{2}C\left(V_{peak}^2 - V_{min}^2\right) = P\Delta t \ , \tag{1}$$

where V_{peak} and V_{min} are the peak and minimum capacitor voltages in Figure 3, and P is the DC load power (approx. constant). From (1),

$$V_{peak}^2 - V_{min}^2 = \frac{2P\Delta t}{C} \ .$$

Factoring the quadratic yields

$$(V_{peak} - V_{min})(V_{peak} + V_{min}) = \frac{2P\Delta t}{C} \ , \text{ or.}$$

$$(V_{peak} - V_{min}) = \frac{2P\Delta t}{C(V_{peak} + V_{min})} \ . \tag{2}$$

At this point, a helpful simplification can be made if, as shown in Figure 6, the following assumptions are made: 1. the AC sinewave of voltage is approximated as a triangular wave, and 2. a straight line decay of voltage.
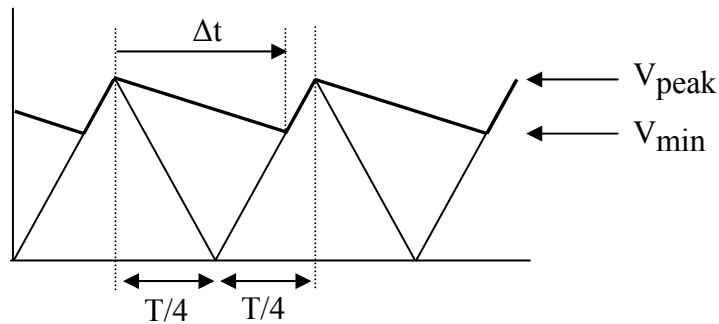
Figure 6. Approximation of Waveform Used for Ripple Calculation Formula

In that case, simple geometry shows the relationship between Δt and $(V_{peak} - V_{min})$ to be

$$\Delta t = \frac{T}{4} + \frac{V_{min}}{V_{peak}} \bullet \frac{T}{4} = \frac{T}{4}\left(1 + \frac{V_{min}}{V_{peak}}\right), \text{ or}$$

$$\Delta t = \frac{T}{4V_{peak}}\left(V_{peak} + V_{min}\right) \ . \tag{3}$$

Substituting into (3) into (2) yields

$$(V_{peak} - V_{min}) = \frac{2P \dfrac{T}{4V_{peak}} \left(V_{peak} + V_{min}\right)}{C(V_{peak} + V_{min})} = \frac{PT}{2CV_{peak}} \quad . \tag{4}$$

Since $T = \dfrac{1}{f}$, then the final expression for ripple becomes

$$(V_{peak} - V_{min}) = V_{peak-to-peak\ ripple} = \frac{P}{2fCV_{peak}} \quad . \tag{5}$$

For the circuit to be built (using 18mF),

$$V_{peak-to-peak\ ripple} \approx \frac{200}{2 \bullet 60 \bullet 18000 \bullet 10^{-6} \bullet 28\sqrt{2}} = 2.33V \quad .$$

Expressed as a percent of peak voltage, the voltage ripple at 200W load is approximately

$$\%V_{ripple} = \frac{V_{peak-to-peak\ ripple}}{V_{peak}} \approx \frac{2.33}{28\sqrt{2}} \bullet 100\% = 5.88\%$$

The Circuit
The schematic for the circuit that you will build is shown in Figure 7. Use a very thin layer of heat sink compound between the diode bridge rectifier module and its heat sink. To maximize effectiveness of the heat sink, make sure that the diode bridge rectifier module has good physical contact with the heat sink and no air gaps in between.

The heat sink should be mounted vertically and held into place by a steel corner bracket so that there is no gap between the heat sink and the wood

Be very careful to connect the polarities of the diode bridge and capacitor. These components can be ruined, and capacitors can explode, if their polarities are reversed!
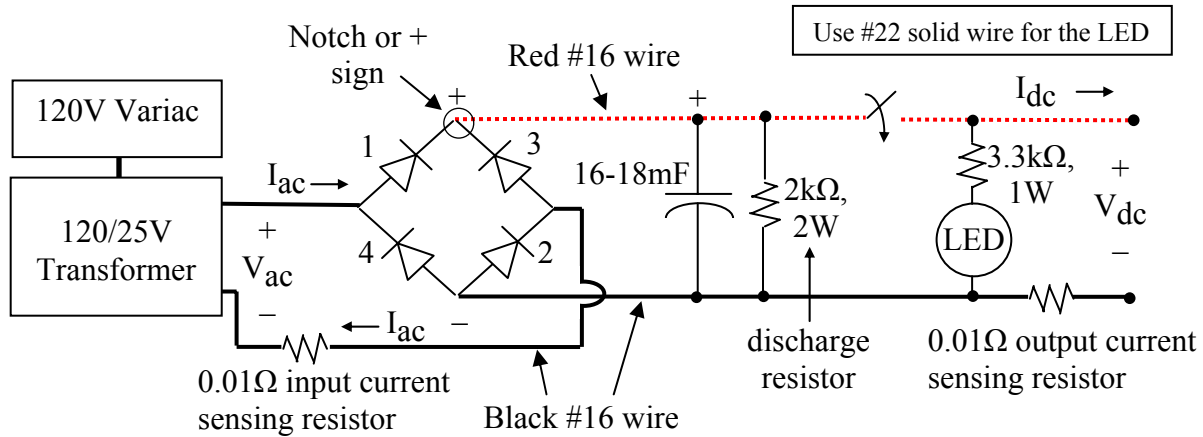
Figure 7. Schematic for Capacitor Filtered Diode Bridge Rectifier
(Note – use the variac to hold $V_{ac} = 28\pm\frac{1}{2}$ Vrms during your experiment. Mount the capacitor vertically. Mount the output switch so that "up" corresponds to the "on" position)

Note – to avoid accidentally shorting the capacitor, never try to measure the voltage directly across the capacitor terminals.

The $2k\Omega$ resistor across the capacitor is a discharge resistor that slowly discharges the capacitor after the circuit is de-energized.

By using the variac to slowly increase input voltage, short circuits or other problems in your circuit can hopefully be identified before damage is done.

Circuit Layout Showing Variac, 25V Transformer, and DBR

Regarding the toggle switch – a hex nut goes on the inside of the steel corner bracket, and the lock washer and round nut go on the outside. Mount the hex nut so that it does not touch the body of the toggle switch. That way, when tightening, the pressure is on the hex nut instead of on the body of the toggle switch (see below)

Space left between hex nut and body of switch
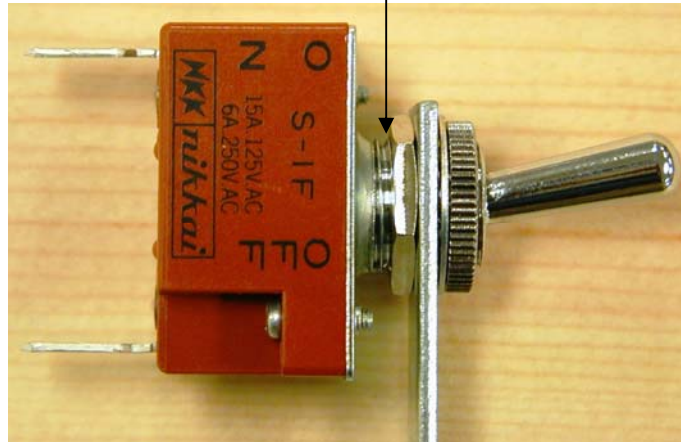
Warning – when connecting quick disconnects to diode bridge rectifier modules and toggle switches, it is very easy to cut your fingers if you are not careful. The proper way is to hold the body of the rectifier module or toggle switch in one hand (or in a vise), and then use your long-nose pliers at a right angle to push the disconnect/wire onto the terminal.
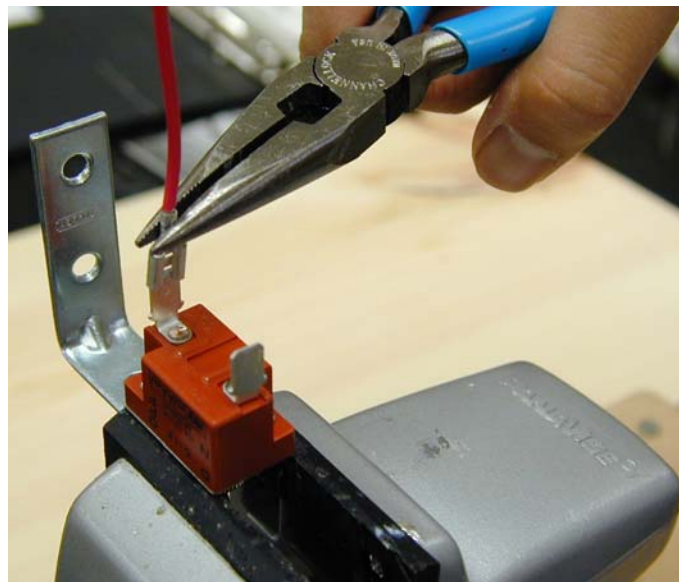
The Experiment

A. **No Load Conditions.** Connect a 25V transformer to the input of your unloaded DBR. Then, with a **variac turned off and its voltage control knob at zero,** plug the 25V transformer into the variac outlet. Slowly raise the variac to a few volts and make sure that the variac current remains zero. Then, slowly raise the variac so that the **transformer output is 28±½ Vrms**. Use a multimeter to measure the "no load" values of V_{ac} and V_{dc}. Make sure you measure V_{dc} at your DBR's output terminals. View no-load V_{ac} on the oscilloscope. Then, move your oscilloscope probe and view no-load V_{dc} on the oscilloscope. The ripple voltage should be nearly zero. **Note – do not attempt to view V_{ac} and V_{dc} simultaneously on the oscilloscope because they have different ground reference points!**

B. **Measure the No Load (Ambient) Temperature of the Heat Sink** using a thermistor (see resistance-temperature characteristics in Table 1) and an ohmmeter. Clamp the thermistor to the top of the heat sink with a wooden clothes pin, so that the thermistor leads point upward. Wait a minute or so for the thermistor temperature to stabilize, and then measure its resistance. An example temperature calculation is shown below the table. Compare your thermistor temperature measurement to that read by one of the infrared thermometers (see a TA or Dr. Grady).
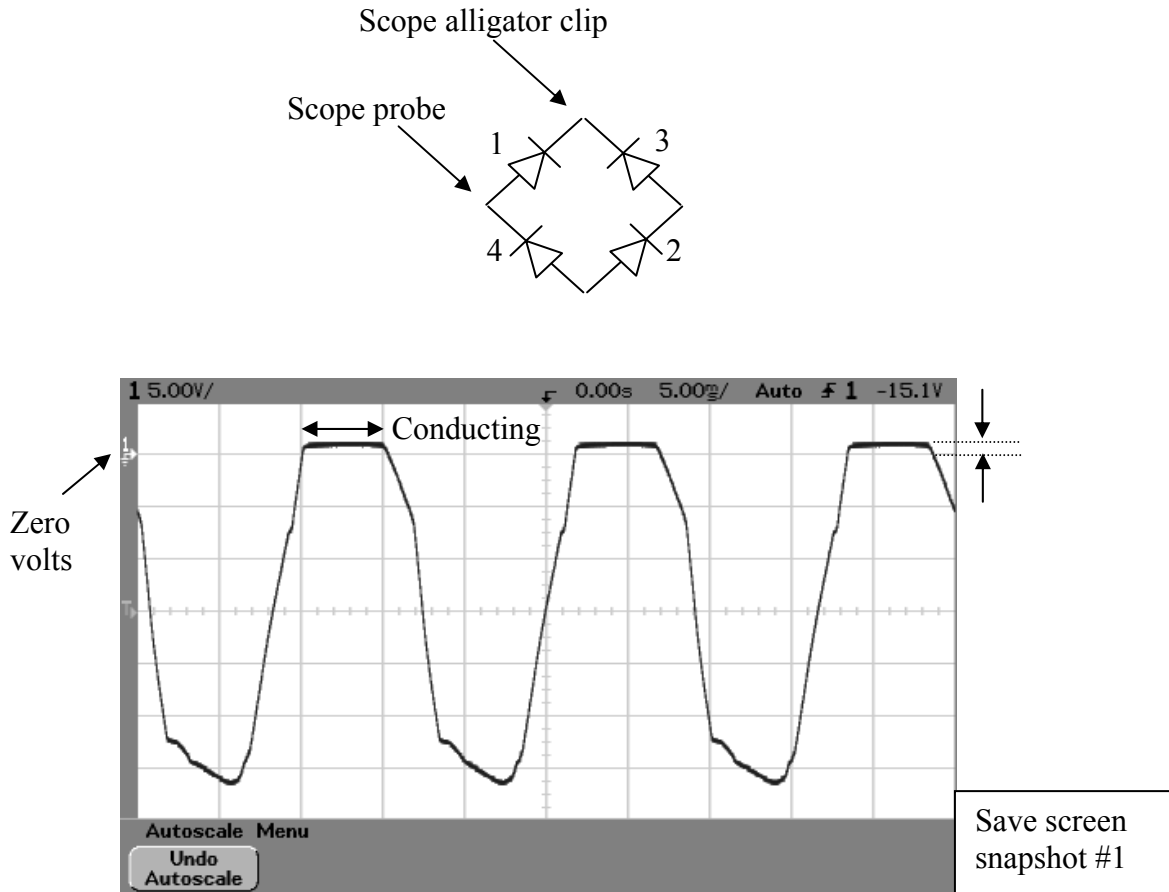
Table 1: Resistance-Temperature Characteristics of GE MTC Thermistors, Negative Temperature Coefficient Thermistor Material Type D9.7A (source www.gesensinginspection.com/en/temperature.html)

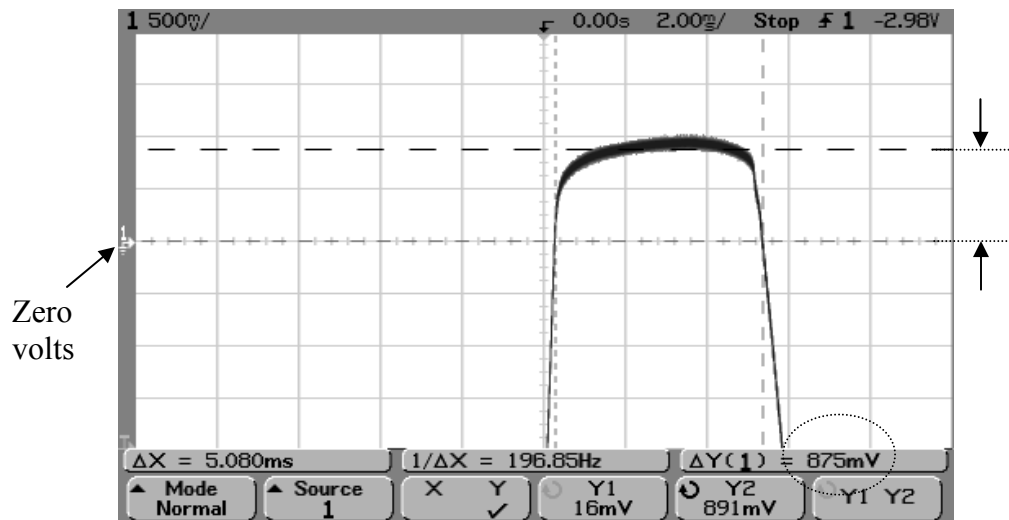| Temp T - °C	RT/R(T=25 °C)	Temp T - °C	RT/R(T=25 °C)
0	3.28	60	0.249
5	2.55	65	0.208
10	1.993	70	0.1752
15	1.573	75	0.1482
20	1.250	80	0.1258
25	1.000	85	0.1073
30	0.806	90	0.0919
35	0.653	95	0.0790
40	0.532	100	0.0682
45	0.437	105	0.0591
50	0.360	110	0.0513
55	0.298		

Example calculation: If the resistance of a 1kΩ (at 25ºC) thermistor is 360Ω, then the thermistor temperature is 50ºC. If the thermistor resistance is 1993Ω, then the thermistor temperature is 10ºC. Use linear interpolation between points. Unlike most materials, the resistance of a thermistor decreases with temperature. This property is used to trigger relays for hot warning lights and motor overheat protection.

Thermistor Resistance
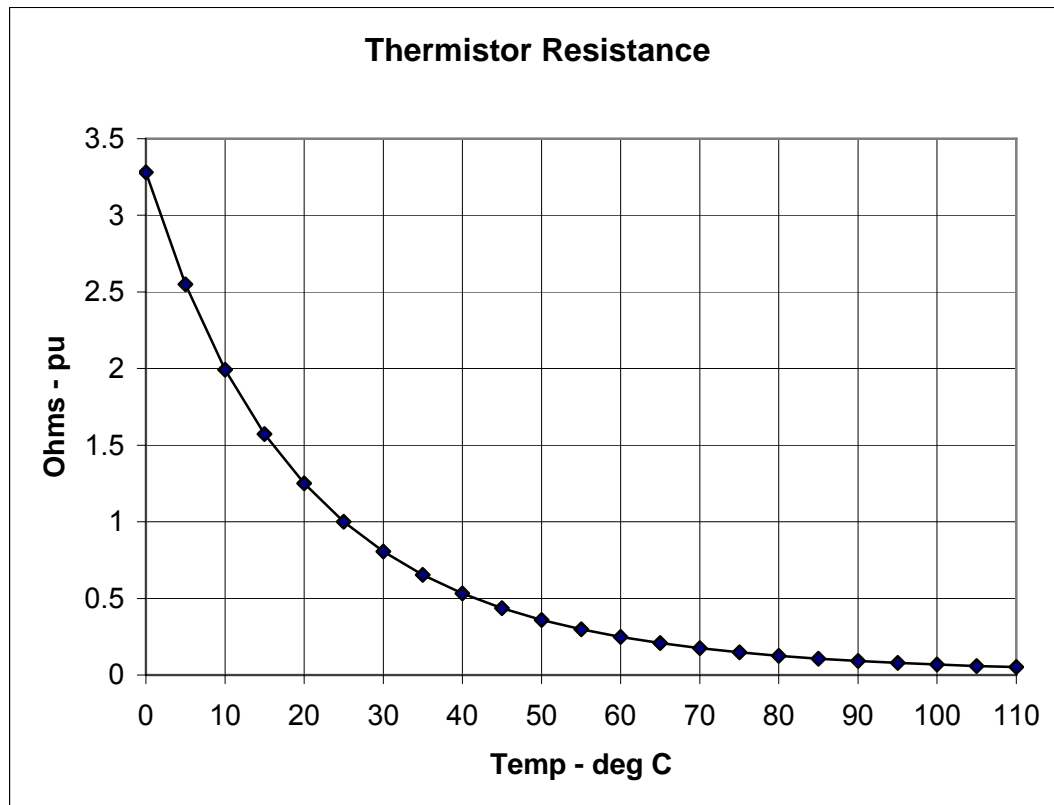
C. **10 Ω Load Resistance.** Connect one 10 Ω or two series 5 Ω, 225W, power resistors to your DBR's output. Raise the variac to hold V_{ac} constant. Use a multimeter to measure V_{ac}, I_{ac} (using the voltage across the **body** of your 0.01Ω input resistor, excluding any extra wiring and contact resistance), V_{dc}, and I_{dc} (using the **body** of your 0.01Ω output resistor). Compute $P_{dc} = V_{dc} \cdot I_{dc}$. View V_{dc} on an oscilloscope, and use the oscilloscope to measure V_{peak} and the peak-to-peak ripple voltage.

D. **5 Ω Load.** Repeat Step C, with one 5 Ω or two parallel 10 Ω, 225W resistors.

E. **Diode Losses and Heat Sink Performance.** For the load condition in Step D, use an oscilloscope to view the forward voltage across one of the diodes in the bridge module. As illustrated on the following page, estimate the average forward voltage drop on the diode during its conduction interval.

Scope alligator clip

Scope probe

1   3

4   2

Conducting

Zero volts

1 5.00V/   0.00s   5.00⁓/   Auto ⨎1 -15.1V

Autoscale Menu
Undo
Autoscale

Save screen snapshot #1

Example for Step E. Connecting the oscilloscope across one diode will display the forward voltage across one diode during conduction. The forward voltage drop is seen to be approximately 1V.


1 500⁓/   0.00s   2.00⁓/   Stop ⨎1 -2.98V

Zero volts

ΔX = 5.080ms   1/ΔX = 196.85Hz   ΔY(1) = 875mV

Mode   Source   X   Y   Y1   Y2   Y1 Y2
Normal   1   ✓   16mV   891mV

Example for Step E. "Zooming-in" on the forward voltage and using the cursors gives a more accurate reading of the average forward voltage drop. In this case, the average is approximately 0.875V

Next, use the oscilloscope to estimate the average ac current during one conduction pulse. Note – each diode sees one pulse of the ac current, once per cycle. Use the voltage and current averages to compute total average power loss on all four diodes as shown in (6) in the following figure.

Estimate on oscilloscope the average value I_{avg} of ac current over conduction interval T_{cond}

Estimate on oscilloscope the average value V_{avg} of diode forward voltage drop over conduction interval T_{cond}

T_{cond}

Since the forward voltage on the diode is approximately constant during the conduction interval, the energy absorbed by the diode during the conduction interval is approximately $V_{avg} \bullet I_{avg} \bullet T_{cond}$. Each diode has one conduction interval per 60Hz period, so the average power absorbed by all four diodes is then

$$P_{avg} = \frac{4V_{avg}I_{avg}T_{cond}}{T_{60Hz}} = 240V_{avg}I_{avg}T_{cond} \text{ Watts.} \qquad (6)$$

Example for Step E. The AC current is viewed by observing the voltage across the 0.01Ω input current sensing resistor. Use the averaging feature of the scope to "denoise" the waveform and display it properly. Then, "freeze" the waveform. By adjusting the cursors, the period is seen to be approximately 16.72ms (i.e., 1÷60Hz).
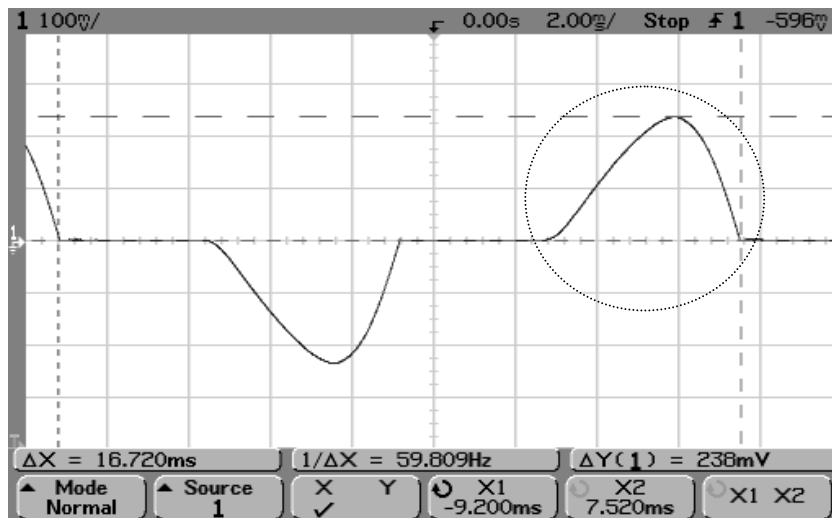
Save screen snapshot #2

One pulse of the AC current passes through each diode pair. In the example shown above, the peak of the voltage pulse across the 0.01Ω current shunt is 238mV, corresponding to $0.238V \div 0.01 = 23.8A$. The conduction time is 4.68ms. Because the pulse is approximately triangular, the average value during conduction is about $23.8 \div 2 = 11.9A$. A handy fact to remember is that with a 0.01Ω current shunt, 10mV corresponds to 1A.

After the circuit has been operating with the 5Ω load for at least five minutes, use a thermistor to measure the temperature of the heat sink. Compute the ºC rise above ambient (note – ambient temperature was measured in Step B). Use the power loss from (6) and the temperature rise to compute the thermal resistance coefficient of the heat sink (in ºC rise per Watt). The manufacturer's catalog thermal resistance value is approximately 2ºC/W. Compare your thermistor temperature measurement to that shown by one of the infrared thermometers.

F. **Plot I_{dc} vs. V_{dc} for Steps A, C, and D.** Put I_{dc} on the vertical axis, and V_{dc} on the horizontal axis.

G. **Plot Measured %V_{ripple} for Steps A, C, and D.** Put %V_{ripple} on the vertical axis, and P_{dc} on the horizontal axis.

H. **Plot Theoretical %V_{ripple} for Steps A, C, and D.** Use (5) with the measured values of V_{peak} and P (i.e., $P = V_{dc} \cdot I_{dc}$). Superimpose the results of (5) on the plot from Step G.

I. **Measurements vs. Theory.** Comment on the differences between Steps G and H.

J. **Estimate the Capacitance of the Electrolytic Capacitor.** Switch off the transformer and connect the scope probes across the 5Ω power resistor. Switch on the transformer. Set the scope vertical axis to 10V/div, and the time axis to 100msec/div. Adjust the scope so that the trace and ground reference are both visible (see below). Set the trigger mode to "normal," and the trigger edge to "downward." Then, switch off the transformer. You should see a response similar to that shown below. The exponential decreases by the factor $e^{-1} = 0.368$ in one time constant $\tau = RC$ seconds. Use the graph, and the known R, to estimate C.
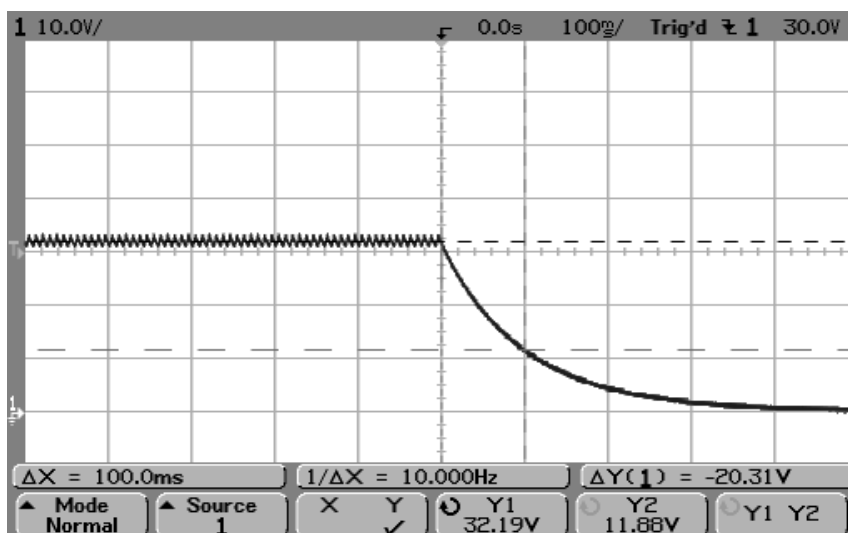
EE462L, Power Electronics, Capacitor Filtered Diode Bridge Rectifier
Version Sept. 8, 2010

Parts List

- Five 2-terminal, 30A terminal blocks (Molex/Beau, Mouser #538-38211-0102)
- 200V, 35A diode bridge rectifier module (Vishay Semiconductor, Mouser #625-GBPC3502-E4), (note + and – terminals, and be careful with polarity!)
- One 3" by 4" heat sink (Wakefield 641K, Mouser #567-641-K, or DigiKey # 345-1053-ND). Hole drilled with 5/32" bit, and de-burred to smooth surface, to fit 1½" steel corner bracket.
- 18000µF, 50V Mallory computer-grade electrolytic capacitor (Mouser #539-CGS50V18000), with screws and lockwashers (note + and – terminals, and be careful with polarity!). Alternatively, use 16000µF, 50V capacitors.
- Vertical mounting clamp with tightening screw for capacitor (For 18,000µF, use Mallory VR8, Mouser #539-VR8; for 16,000µF, use Mallory VR3, Mouser #539-VR3), or equivalent. (Clamp uses #6-32 x ½" to 1" machine screw and nut)
- Toggle switch, SPST, 125V, 15A with quick connect terminals (Mouser #633-S1F-RO)
- GE NTC thermistors, 1kΩ at 25ºC (Mouser #527-2004-1K). Alternately, use 500Ω or 2kΩ.
- Wooden clothes pin to hold the thermistor firmly against heat sink fins to make a good thermal contact.
- LED indicator light and assembly, T-1¾ (5mm), approx. 10ma (Mouser #358-R9-104L-12-R)
- 1½" steel corner bracket for mounting the heat sink (Stanley 30-3170, Home Depot).
- 2" steel corner bracket for mounting the switch (Stanley 30-3300, Home Depot). Hole in bracket enlarged with 15/32" drill bit to fit the toggle switch.
- 1" steel corner bracket for mounting LED. Hole in bracket enlarged with 5/16" drill bit to fit the LED indicator assembly.
- Two 0.01Ω, 3W metal element current sensing resistors (IRC Advanced Film Division, Mouser #66-LOB3R010JLF), or (Ohmite, Digikey #630HR010-ND) (in student parts bin)
- 2kΩ, 2W resistor (in student parts bin)
- 3.3kΩ, 1W resistor (in student parts bin)
- 1" x 6" wood (approx. 12" long piece)

Plastic bags for parts

- 6"x6", 4mil for small parts
- 8"x10", 6mil for holding everything

#8-32, 1" machine screw, flat washer,
split washer, and hex nut for mounting
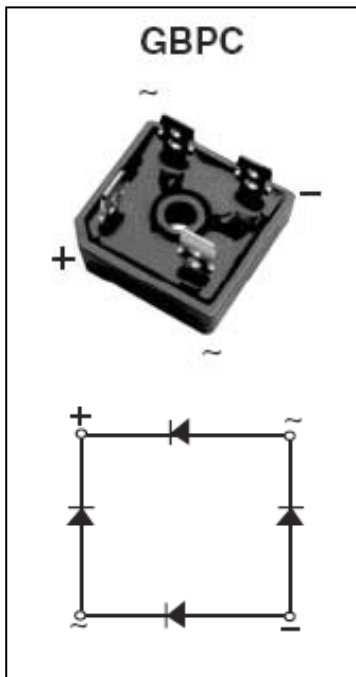DBR module to heat sink
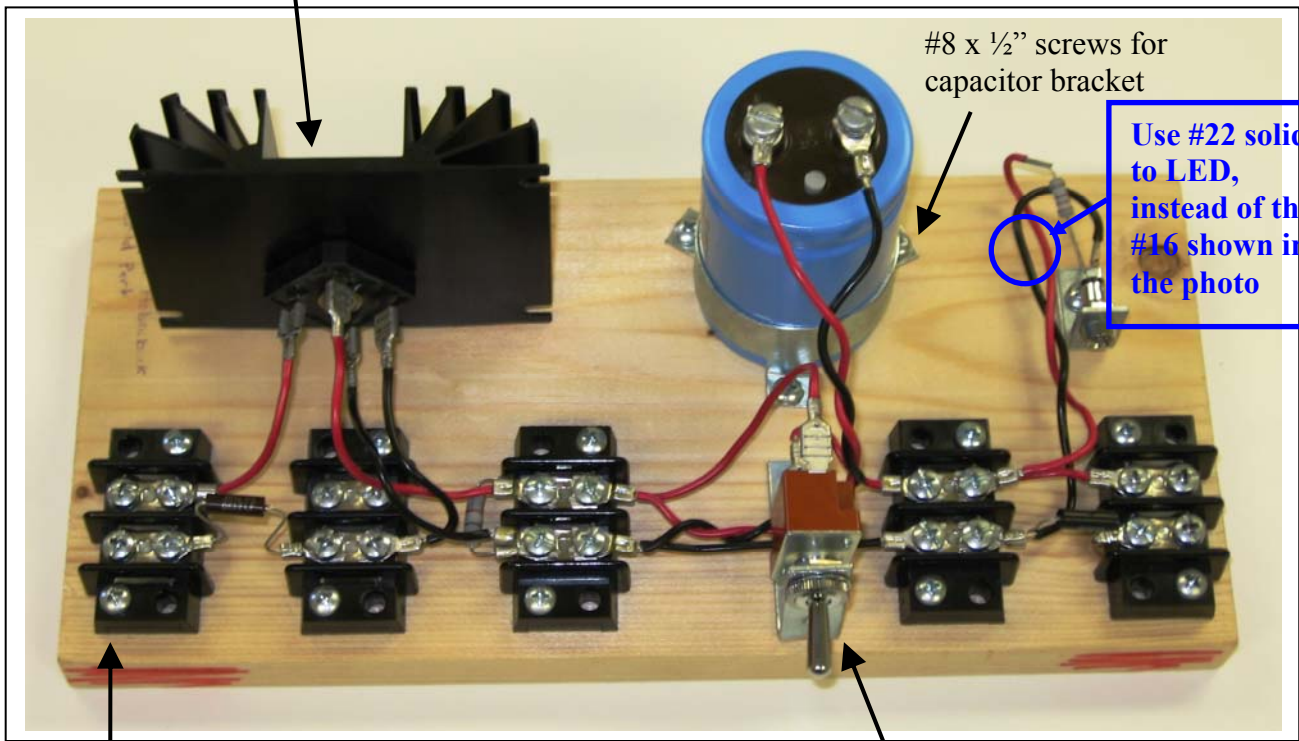
#8 x ½" screws for
capacitor bracket

**Use #22 solid
to LED,
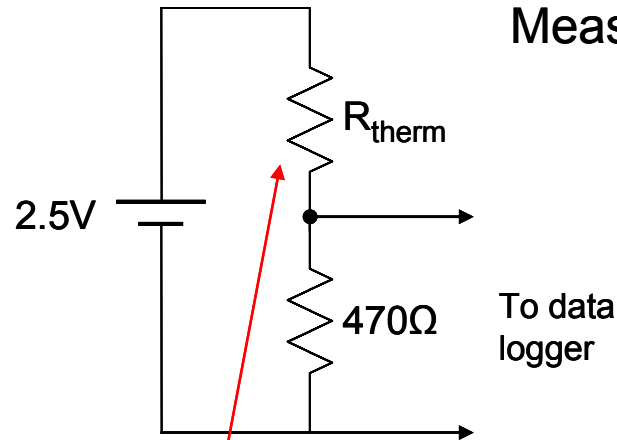instead of the
#16 shown in
the photo**

#8 x 3/4" screws for
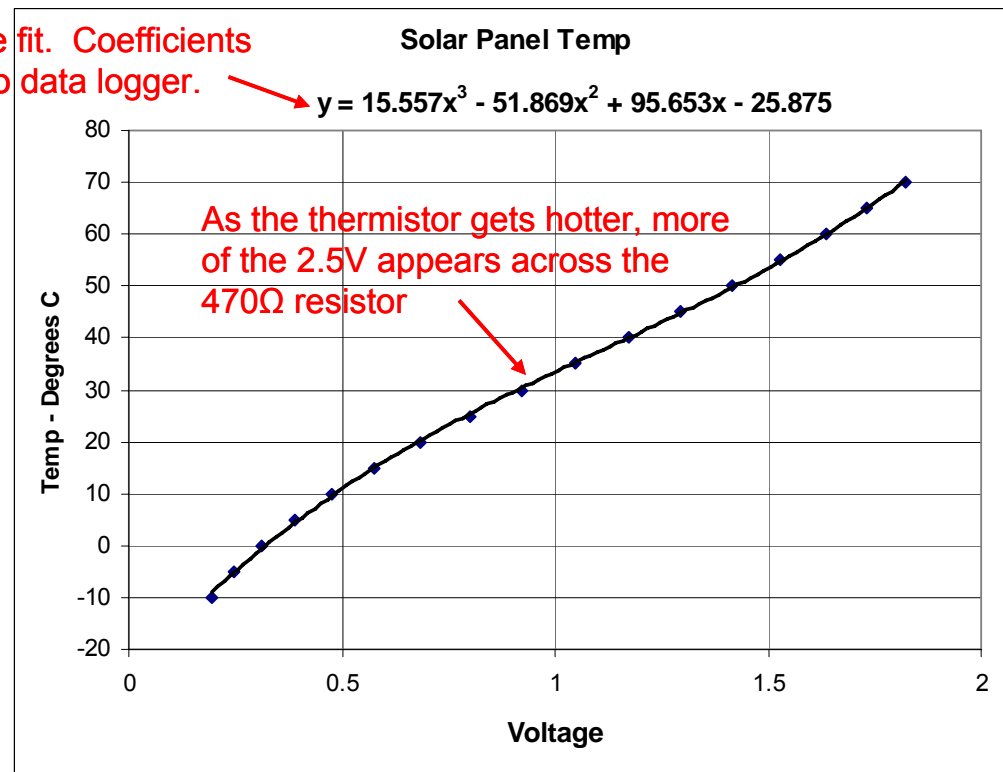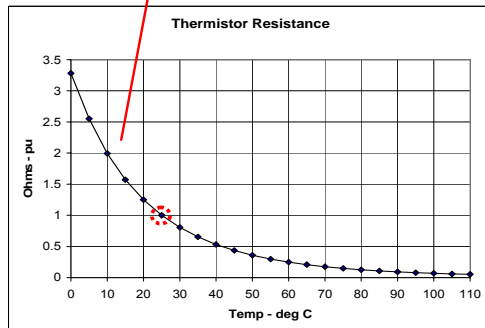terminal blocks

#8 x ½" screws for
corner brackets

200V, 35A Vishay Semicondutor
DBR Module

Measuring the temperature on the backside of a solar panel

R_{therm}

2.5V

470Ω

To data logger

- Thermistor in series with 470Ω resistor

- Series combination energized by 2.5Vdc

- The voltage across the 470Ω resistor then changes with temperature as shown below

Excel curve fit. Coefficients entered into data logger.

Thermistor Resistance

Ohms - pu

Temp - deg C

Solar Panel Temp

$y = 15.557x^3 - 51.869x^2 + 95.653x - 25.875$

Temp - Degrees C

As the thermistor gets hotter, more of the 2.5V appears across the 470Ω resistor

Voltage

EE462L, Power Electronics, Solar Power, I-V Characteristics
Version September 13, 2010

Report Details

Choose any of the solar stations, but take your measurements only when the short circuit current is at least 3.5A. The weather forecast from www.weatherunderground.com can help you plan your schedule.

Your report should include graphs of I versus V, and P versus V. Both actual data and Excel approximations should be plotted together. When plotting with Excel, be sure to use the "scatter plot" option so that the non-uniform spacing between voltage points on the x-axis show correctly. You should also work out numerical values for Equations (1) – (10) for the day and time of your measurements.

Overview

Incident sunlight can be converted into electricity by photovoltaic conversion using a solar panel. A solar panel consists of individual cells that are large-area semiconductor diodes, constructed so that light can penetrate into the region of the p-n junction. The junction formed between the n-type silicon wafer and the p-type surface layer governs the diode characteristics as well as the photovoltaic effect. Light is absorbed in the silicon, generating both excess holes and electrons. These excess charges can flow through an external circuit to produce power.
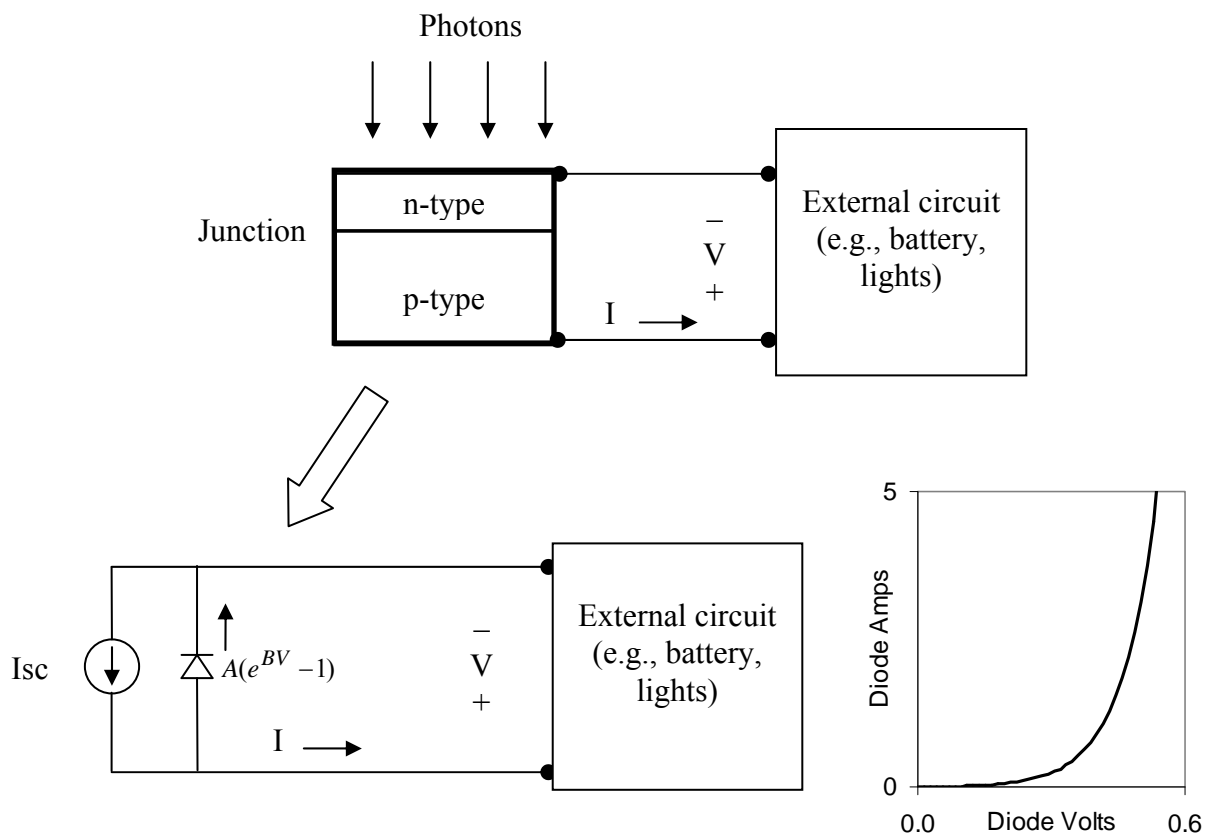
Figure 1. Equivalent Circuit of a Solar Cell

Diode current $A(e^{BV} - 1)$ comes from the standard I-V equation for a diode, plotted above. From Figure 1, it is clear that the current I that flows to the external circuit is

$I = I_{sc} - A(e^{BV} - 1)$. If the solar cell is open circuited, then all of the I_{sc} flows through the diode and produces an open circuit voltage of about 0.5-0.6V. If the solar cell is short circuited, then no current flows through the diode, and all of the I_{sc} flows through the short circuit.

Since the V_{OC} for one cell is approximately 0.5-0.6V, then individual cells are connected in series as a "solar panel" to produce more usable voltage and power output levels. Most solar panels are made to charge 12V batteries and consist of 36 individual cells (or units) in series to yield panel $V_{OC} \approx 18$-20V. The voltage for maximum panel power output is usually about 16-17V. Each 0.5-0.6V series unit can contain a number of individual cells in parallel, thereby increasing the total panel surface area and power generating capability.
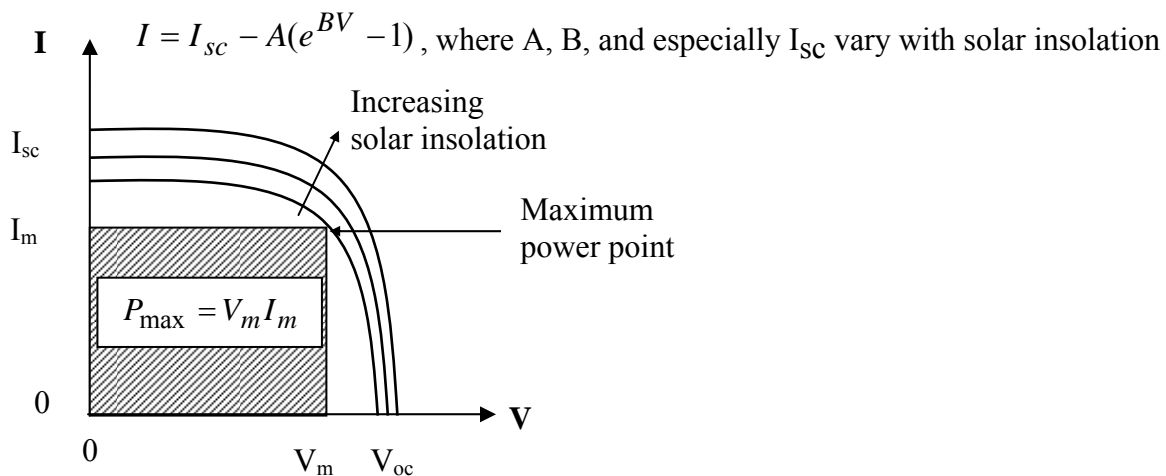
Figure 2. I-V Characteristics of Solar Panel

On a clear day, direct normal solar insolation (i.e., incident solar energy) is approximately $1kW/m^2$. Since solar panel efficiencies are approximately 14%, a solar panel will produce about 140W per square meter of surface area when facing a bright sun. High temperatures reduce panel efficiency. For 24/7 power availability, solar power must be stored in deep-discharge batteries that contain enough energy to power the load through the nighttime and overcast days. On good solar days in Austin, you can count on solar panels producing about 1kWH of energy per square meter.

An everyday use of solar power is often seen in school zone and other LED flashing signs, where TxDOT and municipal governments find them economical when conventional electric service is not readily available or when the monthly minimum electric fees are large compared to the monthly kWH used. Look for solar panels on top of these signs, and also note their orientation.

The Solar Panels on ENS Rooftop
The ENS rooftop is equipped with six pairs of commercial "12V class" panels, plus one larger "24V class" commercial panel. The panels are:
- three pair of British Petroleum BP585, (mono-crystalline silicon, laser grooved, **each panel** 85W, voltage at maximum power = 18.0V, current at maximum power = 4.7A, open circuit voltage = 22.3V, short circuit current = 5.0A). These three pairs are connected to ENS212 stations 17, 18, and 19.
- two pair of Solarex SX85U (now BP Solar) (polycrystalline silicon, **each panel** 85W, voltage at maximum power = 17.1V, current at maximum power = 5.0A, open circuit voltage = 21.3V, short circuit current = 5.3A). These two pairs are connected to ENS212 stations 15 and 16.
- one pair of Photowatt PW750-80 (multi-crystalline cells, **each panel** 80W, voltage at maximum power = 17.3V, current at maximum power = 4.6A, open circuit voltage = 21.9V, short circuit current = 5.0A). This pair is connected to ENS212 station 21.
- one British Petroleum BP3150U, 150W panel (multicrystalline), open circuit voltage = 43.5V, short circuit current = 4.5A. This is connected to ENS212 station 20.

Each of the seven stations is wired to ENS212 and has an open circuit voltage of approximately 40V and a short circuit current of approximately 5A. The I-V and P-V characteristics for one of the panel pairs is shown in Figure 3. The I-V curve fit equation for Figure 3 is

$$I(V) = 5.34 - 0.00524 \left(e^{0.1777V} - 1 \right).$$

PV Station, Bright Sun

PV Station, Bright Sun
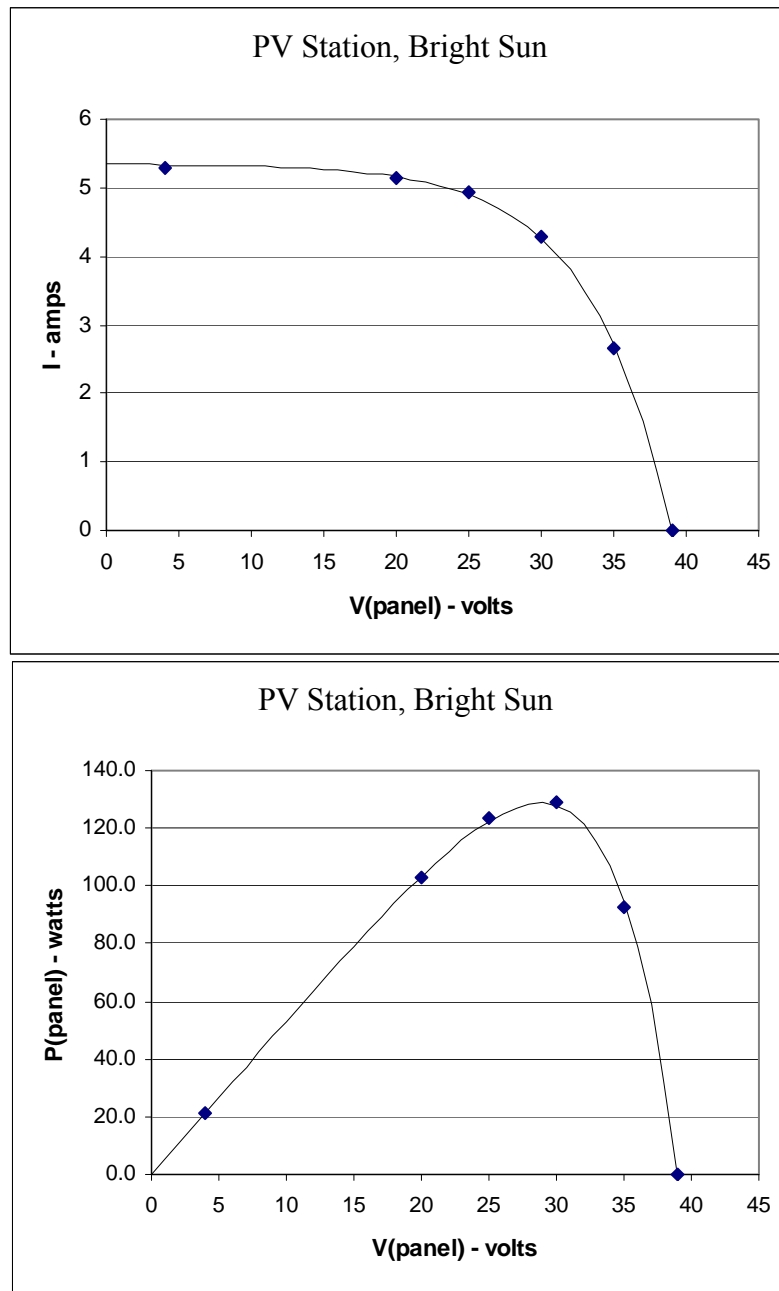
Figure 3. I-V and P-V Characteristics for One of the Panel Pairs
(data points taken by loading the panel pair with a variable load resistor)

Maximum Power
As seen in bottom figure of Figure 3, panels have a maximum power point. Maximum power
corresponds to V_m and I_m in Figure 2. Because solar power is relatively expensive (approx. $4-
5 per watt for the panels, plus the same amount for batteries and electronics), it is important to
operate panels at their maximum power conditions. Unfortunately, V_m, I_m, and the Thevenin

equivalent resistance vary with light level. DC-DC converters are often used to "match" the load resistance to the Thevenin equivalent resistance of the panel to maximize the power drawn from the panel. These "smart" converters (often referred to as "tracking converters") also charge the storage batteries in such a way as to maximize battery life.

Sun Position, Panel Orientation, and PV Harvest – The Big 10 Equations
Ideally, a solar panel should track the sun so that the incident solar rays are perpendicular to the panel surface, thus maximizing the capture of solar energy. However, because of high wind loads, most panels are fixed in position. Often, panel tilt (with respect to horizontal) is adjusted seasonally. Orientation of fixed panels should be carefully chosen to capture the most energy for the year, or for a season.

The position of the sun in the sky varies dramatically with hour and season. Sun zenith angle θ_{sun}^{zenith} is expressed in degrees from vertical. Sun azimuth $\phi_{sun}^{azimuth}$ is expressed in degrees from true north. Sun zenith and azimuth angles are illustrated in Figure 4.
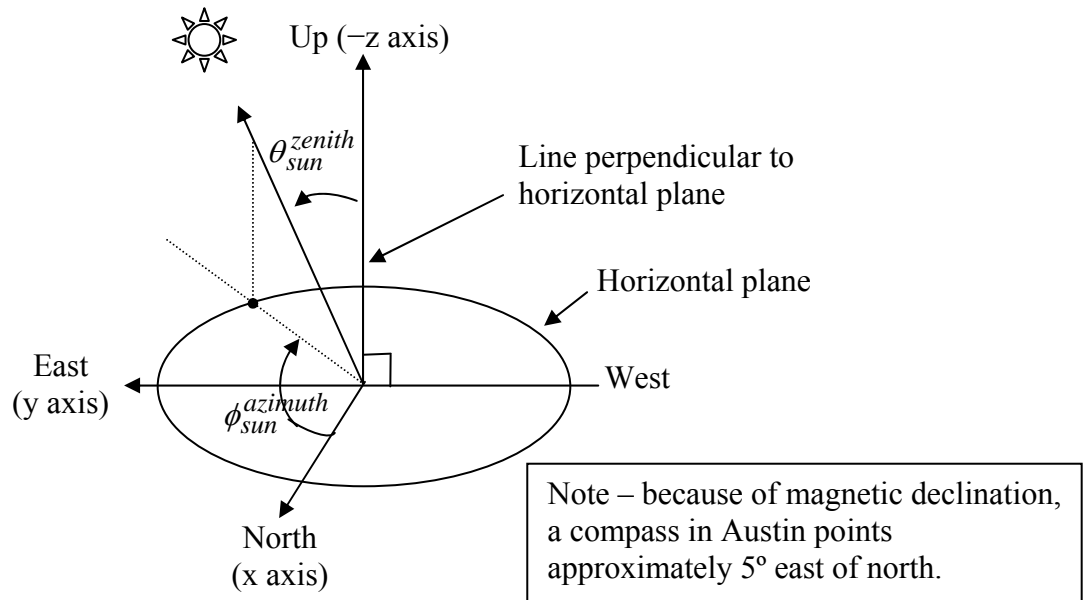
Figure 4. Sun Zenith and Azimuth Angles

Sun position angles are available in many references, and with different levels of complexity. Some of the following equations were taken from the University of Oregon Solar Radiation Monitoring Laboratory (http://solardat.uoregon.edu/SolarRadiationBasics.html):

Sun declination angle (in degrees) is

$$\delta = 23.45\sin(B), \text{ where}$$

$$B = \frac{360}{365}(n-81) \text{ degrees , and}$$

n = day of year (i.e., 1,2,3, … , 364,365). **(1)**

First Day of	n	First Day of	n
January	1	July	182+
February	32	August	213+
March	60+	September	244+
April	91+	October	274+
May	121+	November	305+
June	152+	December	335+

+ add 1 for leap years

Equation of time (in decimal minutes) is

$$E_{qt} = 9.87\sin(2B) - 7.53\cos(B) - 1.5\sin(B). \qquad \textbf{(2)}$$

Solar time (in decimal hours) is

$$T_{solar} = T_{local} + \frac{E_{qt}}{60} + \frac{\left(Longitude_{timezone} - Longitude_{local}\right)}{15}, \qquad \textbf{(3)}$$

where

- T_{local} is local standard time in decimal hours,

- $Longitude_{timezone}$ is the longitude at the eastern edge of the time zone (e.g., $90°$ for Central Standard Time).

(Note – in the Solar_Data_Analyzer Excel spreadsheet program, $\left(Longitude_{timezone} - Longitude_{local}\right)$ is entered as "Longitude shift (deg)." At Austin, with $Longitude_{local} = 97.74°$, the longitude shift is $(90° - 97.74°) = -7.74°$.

Hour angle (in degrees) is

$$H = 15 \bullet \left(12 - T_{solar}\right). \qquad \textbf{(4)}$$

Cosine of the zenith angle is

$$\cos\left(\theta_{sun}^{zenith}\right) = \sin(L)\sin(\delta) + \cos(L)\cos(\delta)\cos(H), \qquad \textbf{(5)}$$

where L is the latitude of the location.

Solar azimuth comes from the following calculations. Using the formulas for solar radiation on tilted surfaces, consider vertical surfaces directed east and south. The fraction of direct component of solar radiation on an east-facing vertical surface is

$$f_{VE} = \cos(\delta)\sin(H). \qquad \textbf{(6)}$$

The fraction of direct component of solar radiation on a south-facing vertical surface is

$$f_{VS} = -\sin(\delta)\cos(L) + \cos(\delta)\sin(L)\cos(H). \qquad \textbf{(7)}$$

Equations (6) and (7) correspond to the projections, on the horizontal plane, of a vector pointing toward the sun. By examining Figure 4, $\phi_{sun}^{azimuth}$ can be found as follows:

$$\text{If } f_{VE} \geq 0, \ \phi_{sun}^{azimuth} = \cos^{-1}\left(\frac{-f_{VS}}{\sqrt{f_{VE}^2 + f_{VS}^2}}\right) \text{ degrees,}$$

$$\text{If } f_{VE} < 0, \ \phi_{sun}^{azimuth} = 180 + \cos^{-1}\left(\frac{f_{VS}}{\sqrt{f_{VE}^2 + f_{VS}^2}}\right) \text{ degrees.} \tag{8}$$

As a check, all components of the sun radiation should account for the total, i.e.

$$\sqrt{f_{VE}^2 + f_{VS}^2 + \cos^2\left(\theta_{sun}^{zenith}\right)} = 1.$$

Illustrations of seasonal and daily sun positions for Austin are shown in Figures 5a and 5b.

An example of the step-by-step calculations for 3pm (i.e., 15.00 decimal hours) on October 25th in Austin follows.

Input	$n = 298^{th}$ day
Compute	$B = 214.0°$
Compute	$\delta = -13.11°$
Compute	$E_{qt} = 16.21$ decimal minutes
Input	Longitude $= 97.74°$
Input	Longitude shift $= -7.74°$
Input	$T_{local} = 15.00$ decimal hours
Compute	$T_{solar} = 14.75$ decimal hours
Compute	$H = -41.25°$
Input	Latitude (L) $= 30.29°$
Compute	$\theta_{sun}^{zenith} = 58.81°$ ← output
Compute	$f_{VE} = -0.6421$
Compute	$f_{VS} = 0.5651$
Compute	$\phi_{sun}^{azimuth} = 228.7°$ ← output

Solar Zenith versus Azimuth at Austin
22nd Day of Dec, Jan, Feb, Mar, Apr, May, Jun
(Sun hrs/day. Dec=10.0,Jan=10.3,Feb=11.0,Mar=12.0,Apr=12.8,May=13.6,Jun=13.9)

Azimuth (South = 180)
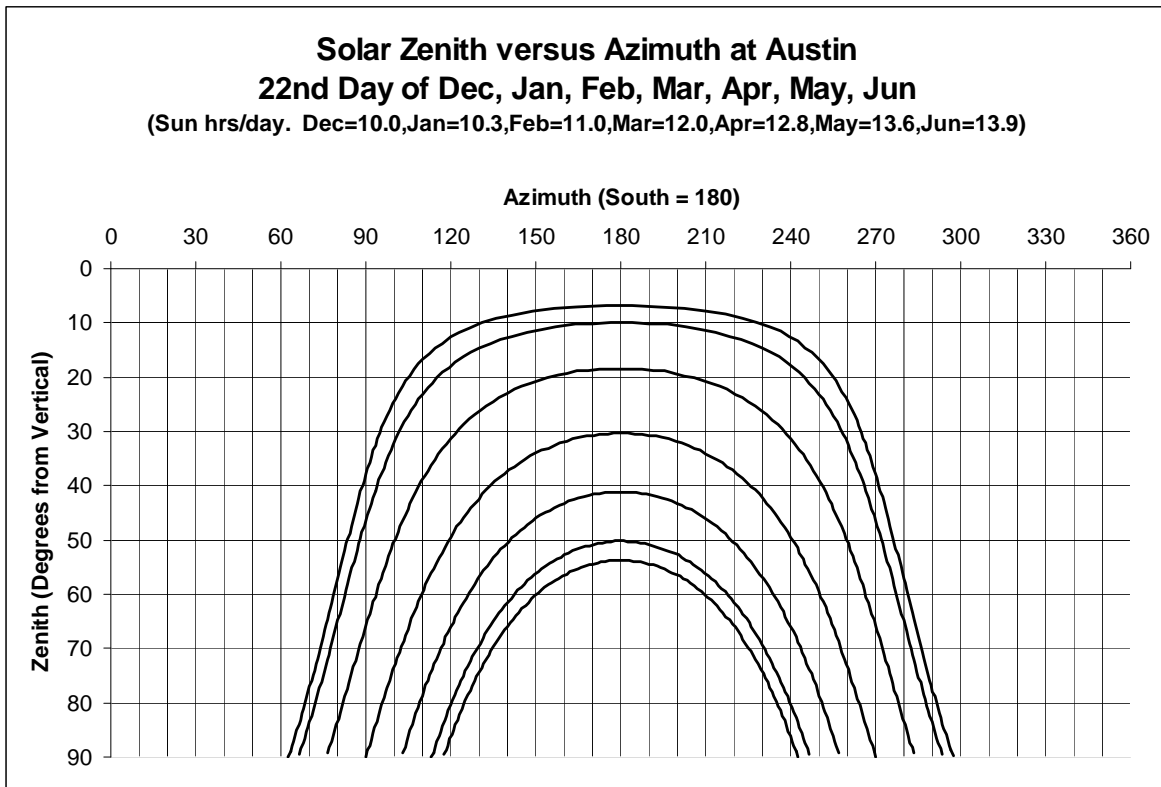
Figure 5a. Sun Position for Winter and Spring Seasons in Austin
(note – solar noon in Austin occurs at approximately 12:30pm CST)

Solar Zenith versus Azimuth at Austin
22nd Day of Jun, Jly, Aug, Sep, Oct, Nov, Dec
(Sun hrs/day. Jun=13.9,Jly=13.6,Aug=12.8,Sep=12.0,Oct=11.0,Nov=10.3,Dec=10.0)

Azimuth (South = 180)
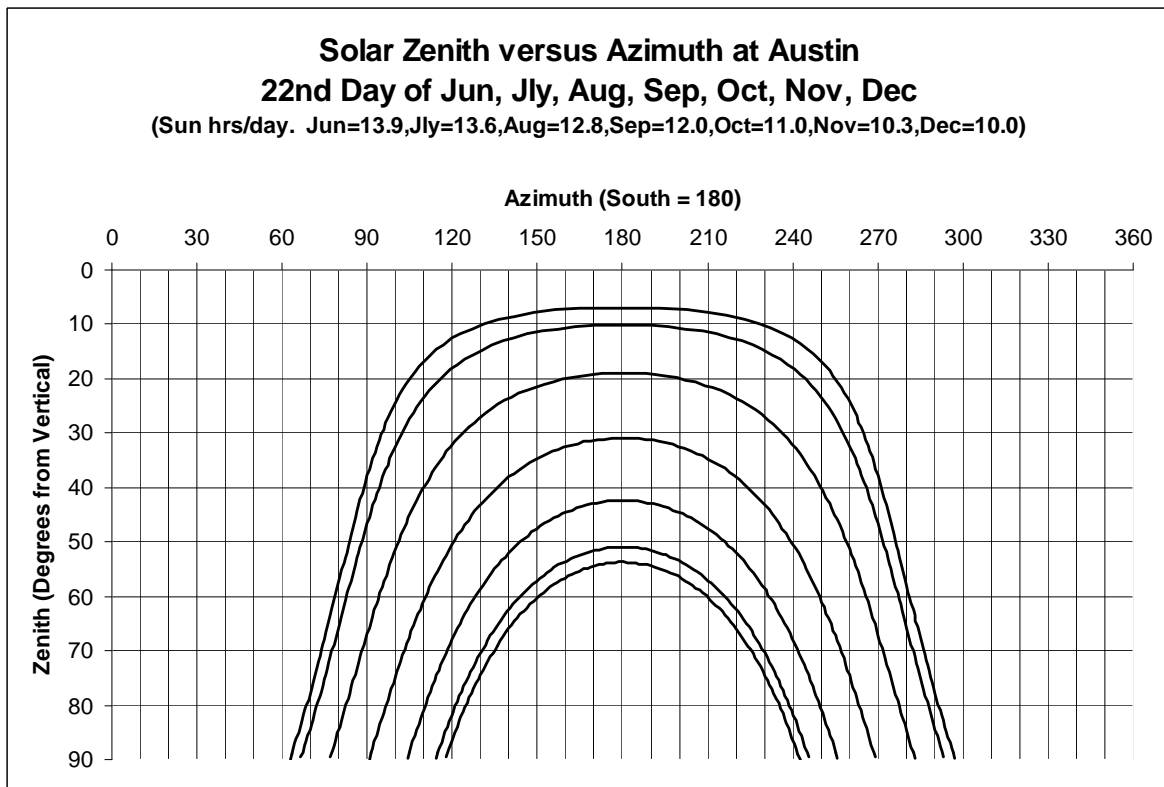
Figure 5b. Sun Position for Summer and Fall Seasons in Austin
(note – solar noon in Austin occurs at approximately 12:30pm CST)

Definitions from www.weatherground.com

Twilight	This is the time before sunrise and after sunset where it is still light outside, but the sun is not in the sky.
Civil Twilight	This is defined to be the time period when the sun is no more than 6 degrees below the horizon at either sunrise or sunset. The horizon should be clearly defined and the brightest stars should be visible under good atmospheric conditions (i.e. no moonlight, or other lights). One still should be able to carry on ordinary outdoor activities.
Nautical Twilight	This is defined to be the time period when the sun is between 6 and 12 degrees below the horizon at either sunrise or sunset. The horizon is not defined and the outline of objects might be visible without artificial light. Ordinary outdoor activities are not possible at this time without extra illumination.
Astronomical Twilight	This is defined to be the time period when the sun is between 12 and 18 degrees below the horizon at either sunrise or sunset. The sun does not contribute to the illumination of the sky before this time in the morning, or after this time in the evening. In the beginning of morning astronomical twilight and at the end of astronomical twilight in the evening, sky illumination is very faint, and might be undetectable.
Length Of Day	This is defined to be the time of Actual Sunset minus the time of Actual Sunrise. The change in length of daylight between today and tomorrow is also listed when available.
Length Of Visible Light	This is defined to be the time of Civil Sunset minus the time of Civil Sunrise.
Altitude (or Elevation)	First, find your azimuth. Next, the Altitude (or elevation) is the angle between the Earth's surface (horizon) and the sun, or object in the sky. Altitudes range from -90° (straight down below the horizon, or the nadir) to +90° (straight up above the horizon or the Zenith) and 0° straight at the horizon.
Azimuth	The azimuth (az) angle is the compass bearing, relative to true (geographic) north, of a point on the horizon directly beneath the sun. The horizon is defined as an imaginary circle centered on the observer. This is the 2-D, or Earth's surface, part of calculating the sun's position. As seen from above the observer, these compass bearings are measured clockwise in degrees from north. Azimuth angles can range from 0 - 359°. 0° is due geographic north, 90° due east, 180° due south, and 360 due north again.

Hour Angle of the Sun	The Solar Hour Angle of the Sun for any local location on the Earth is zero° when the sun is straight overhead, at the zenith, and negative before local solar noon and positive after solar noon. In one 24-hour period, the Solar Hour Angle changes by 360 degrees (i.e. one revolution).
Mean Anomaly of the Sun	The movement of the Earth around the Sun is an ellipse. However, if the movement of the Earth around the Sun were a circle, it would be easy to calculate its position. Since, the Earth moves around the sun about one degree per day, (in fact, it's 1/365.25 of the circle), we say the Mean Anomaly of the Sun is the position of the Earth along this *circular* path. The True Anomaly of the Sun is the position along its real elliptical path.
Obliquity	Obliquity is the angle between a planet's equatorial plane and its orbital plane.
Right Ascension of the Sun	The Celestial Sphere is a sphere where we project objects in the sky. We project stars, the moon, and sun, on to this imaginary sphere. The Right Ascension of the Sun is the position of the sun on our Celestial Sphere
Solar Noon (and Solar Time)	Solar Time is based on the motion of the sun around the Earth. The apparent sun's motion, and position in the sky, can vary due to a few things such as: the elliptical orbits of the Earth and Sun, the inclination of the axis of the Earth's rotation, the perturbations of the moon and other planets, and of course, your latitude and longitude of observation. Solar Noon is when the sun is at the highest in the sky, and is defined when the Hour Angle is 0°. Solar Noon is also the midpoint between Sunrise and Sunset.
Sun Declination	The Declination of the sun is how many degrees North (positive) or South (negative) of the equator that the sun is when viewed from the center of the earth. The range of the declination of the sun ranges from approximately +23.5° (North) in June to -23.5° (South) in December.

Panel Orientation and Solar Incident Angle
Unless there are obstructions, panels should face due south (i.e., have an azimuth angle of 180º).
Recommended panel tilt angles (above horizontal) are latitude + 15º in winter, and latitude – 15º
in summer. In Austin, with latitude = 30º, these recommendations correspond to 45º in winter,
and 15º in summer. If no seasonal adjustments are made, then the best fixed panel tilt angle is
latitude (i.e., 30º in Austin). The tilt angles of our panels are adjusted twice each year, at the
spring and fall equinoxes. Our tilt angles are 20º in summer, and 45º in winter.

θ_{panel}^{tilt}

Line perpendicular to horizontal plane

Line perpendicular to panel surface

Edge of panel

θ_{panel}^{tilt}

Horizontal plane
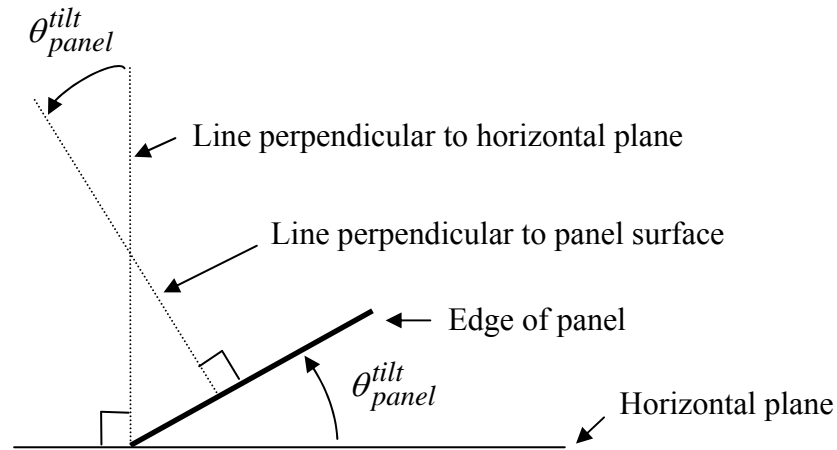
Figure 6. Panel Tilt Angle

Area of each
panel is 0.52m^2

Area of each
panel is 0.54m^2

Area of this
panel is 1.04m^2

Area of each
panel is 0.60m^2

Station 19 BP	Station 17 BP		
Station 21 Photowatt	Station 20 BP	Station 19 BP	Station 17 BP	Station 16 Solarex	Station 15 Solarex
Station 21 Photowatt		Station 18 BP	Station 18 BP	Station 16 Solarex	Station 15 Solarex
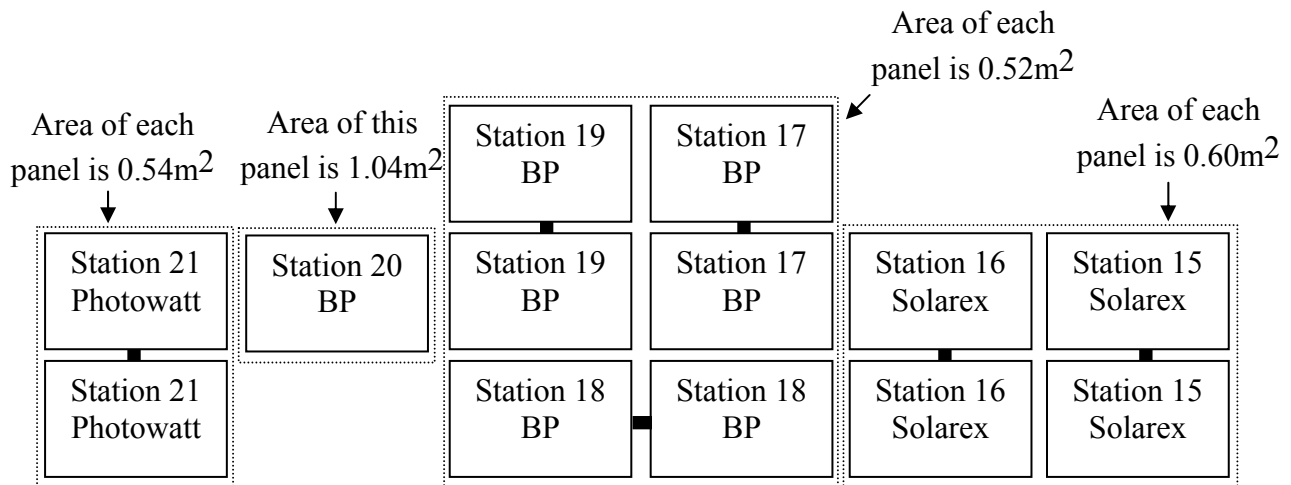
All panels atop ENS have azimuth angle = 190º

View Facing Front of ENS Panels (i.e., looking toward north)
(Note – areas shown are for individual panels, so for a pair, double the values shown)
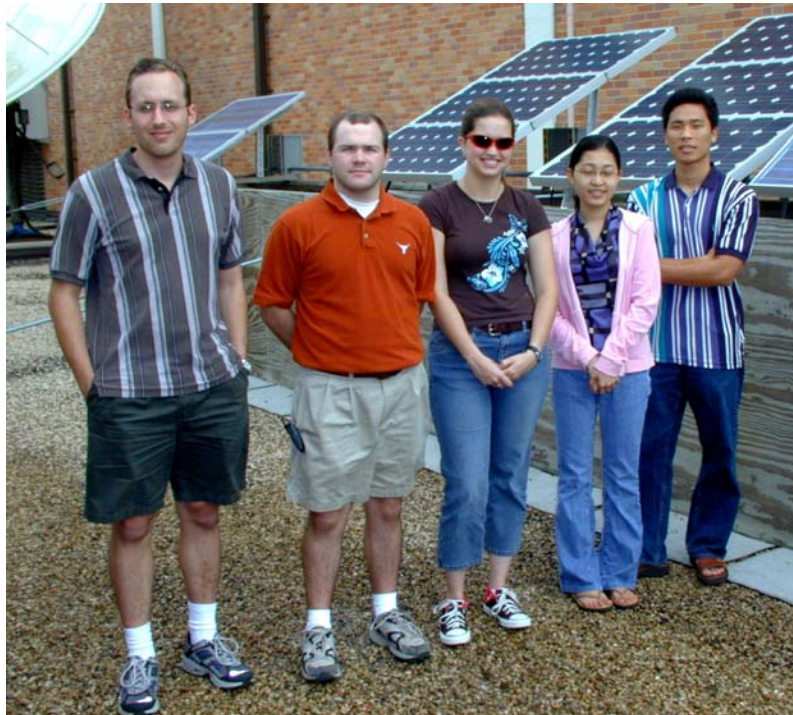
Panels atop ENS

The angle between the rays of the sun and a vector perpendicular to the panel surface is known as the angle of incidence ($\beta_{incident}$). The cosine of $\beta_{incident}$ is found by first expressing a unit vector pointed toward the sun, and a unit vector perpendicular to the panel surface, and then taking the dot product of the two unit vectors. When $\cos(\beta_{incident}) = 1$, then the sun's rays are perpendicular to the panel surface, so that maximum incident solar energy is captured. The expressions follow.

Considering Figure 4, the unit vector pointed toward the sun is

$$\hat{a}_{sun} = \left[\sin\theta_{sun}^{zenith}\cos\phi_{sun}^{azimuth}\right]\hat{a}_x + \left[\sin\theta_{sun}^{zenith}\sin\phi_{sun}^{azimuth}\right]\hat{a}_y - \left[\cos\theta_{sun}^{zenith}\right]\hat{a}_z .$$

Considering Figure 6, the unit vector perpendicular to the panel surface is

$$\hat{a}_{panel} = \left[\sin\theta_{panel}^{tilt}\cos\phi_{panel}^{azimuth}\right]\hat{a}_x + \left[\sin\theta_{panel}^{tilt}\sin\phi_{panel}^{azimuth}\right]\hat{a}_y - \left[\cos\theta_{panel}^{tilt}\right]\hat{a}_z$$

The dot product of the two unit vectors is then

$$\cos\beta_{incident} = \hat{a}_{sun} \bullet \hat{a}_{panel} = \left[\sin\theta_{sun}^{zenith}\cos\phi_{sun}^{azimuth}\sin\theta_{panel}^{tilt}\cos\phi_{panel}^{azimuth}\right]$$

$$+ \left[\sin\theta_{sun}^{zenith}\sin\phi_{sun}^{azimuth}\sin\theta_{panel}^{tilt}\sin\phi_{panel}^{azimuth}\right] + \left[\cos\theta_{sun}^{zenith}\cos\theta_{panel}^{tilt}\right].$$

Combining terms yields

$$\cos\beta_{incident} = \sin\theta_{sun}^{zenith}\sin\theta_{panel}^{tilt}\left[\cos\phi_{sun}^{azimuth}\cos\phi_{panel}^{azimuth} + \sin\phi_{sun}^{azimuth}\sin\phi_{panel}^{azimuth}\right]$$

$$+ \cos\theta_{sun}^{zenith}\cos\theta_{panel}^{tilt} .$$

Simplifying the above equation yields the general case,

$$\cos\beta_{incident} = \sin\theta_{sun}^{zenith}\sin\theta_{panel}^{tilt}\cos\left(\phi_{sun}^{azimuth} - \phi_{panel}^{azimuth}\right) + \cos\theta_{sun}^{zenith}\cos\theta_{panel}^{tilt} . \quad\quad \textbf{(9)}$$

Some special cases are

1. Flat panel (i.e., $\theta_{panel}^{tilt} = 0$). Then,

   $\cos\beta_{incident} = \cos\theta_{sun}^{zenith}$.

2. Sun directly overhead (i.e., $\theta_{zenith}^{sun} = 0$). Then,

$$\cos \beta_{incident} = \cos \theta_{panel}^{tilt} .$$

3. Equal azimuth angles (i.e., azimuth tracking, $\phi_{sun}^{azimuth} = \phi_{panel}^{azimuth}$). Then,

$$\cos \beta_{incident} = \sin \theta_{sun}^{zenith} \sin \theta_{panel}^{tilt} + \cos \theta_{sun}^{zenith} \cos \theta_{panel}^{tilt} = \cos\left(\theta_{sun}^{zenith} - \theta_{panel}^{tilt}\right).$$

4. Sun zenith angle equals panel tilt angle (i.e., zenith tracking, $\theta_{sun}^{zenith} = \theta_{panel}^{tilt}$). Then,

$$\cos \beta_{incident} = \sin^2 \theta_{sun}^{zenith} \cos\left(\phi_{sun}^{azimuth} - \phi_{panel}^{azimuth}\right) + \cos^2 \theta_{sun}^{zenith} .$$

To illustrate the general case, consider the following example: 3pm (standard time) in Austin on October 25. The sun position is

$$\phi_{sun}^{azimuth} = 228.7°, \ \theta_{sun}^{zenith} = 58.8°, \ \text{so that} \ \hat{a}_{sun} = -0.565\hat{a}_x - 0.643\hat{a}_y - 0.517\hat{a}_z ,$$

and the panel angles are

$$\phi_{panel}^{azimuth} = 190°, \ \theta_{panel}^{tilt} = 45°, \ \text{so that} \ \hat{a}_{panel} = -0.696\hat{a}_x - 0.1228\hat{a}_y - 0.707\hat{a}_z .$$

Evaluating the dot product yields $\cos \beta_{incident} = 0.838$, so $\beta_{incident} = 33.1°$.

Solar Radiation Measurements
The three most important solar radiation measurements for studying solar panel performance are global horizontal (GH), diffuse horizontal (DH), and direct normal (DN). GH is "entire sky," including the sun disk, looking straight up. DH is "entire sky," excluding the sun disk, looking straight up. DN is facing directly toward the sun. The units for GH, DH, and DN are W/m^2.

The direct measurement of DN requires a sun tracking device. The Sci Tek 2AP tracker takes DN, GH, and DH readings every five minutes using three separate thermocouple sensors. The DN sensor tracks and sees only the disk of the sun. The GH sensor points straight up and sees the entire sky with sun disk. The DH sensor points straight up, but a shadow ball blocks the disk of the sun, so that it sees entire sky minus sun disk.

Rotating shadowband pyranometers use one PV sensor, pointed straight up, to measure GH and DH every minute, and then save average values every 5 minutes. Once per minute, the shadow band swings over, and when the shadow falls on the sensor, the DH reading is taken. Using GH and DH, the rotating shadow-band pyranometer estimates DN.

Rotating Shadowband Pyranometers

Rotating shadow band pyranometers are simple in that they do not track the sun. Instead, they merely rotate a shadow band every minute across the PV sensor. When there is no shadow on the sensor, the sensor reads GH. When the shadow falls on the sensor, the sensor reads DH.

Computing Incident Solar Power on a Panel Surface
To compute the incident solar power on a panel surface, we assume that the panel captures all of the diffuse horizontal (DH) power, plus the fraction of (GH – DH) that is perpendicular to the panel surface.

$$P_{incident} = DH + \frac{(GH - DH)}{\cos(\theta_{sun}^{zenith})} \bullet \cos(\beta_{incident}) \text{ W/m}^2. \qquad \textbf{(10)}$$

The above value, in W/m^2, is then multiplied by the panel surface area to yield total incident solar power $P_{incident}$. Multiplying by panel efficiency yields maximum expected electrical power output.

Because panels are rated at 1kW/m2, (10) is also the estimated panel W output per kW rated. Integrate over all hours of the day and divide by 1000, and you get estimated kWH output per kW rated (i.e., the PV daily harvest).

To avoid serious overcorrection when the sun is near the horizon, ignore the $\cos(\theta_{sun}^{zenith})$ term when $\theta_{sun}^{zenith} > 85º$. For the 3pm, October 25th example, the readings are $GH = 535W / m^2$, and $DH = 38W / m^2$,

$$P_{incident} = \left[38 + \frac{(535 - 38)}{\cos(58.9°)} \bullet \cos(33.1°) \right] \bullet A_{panel} = 844 \bullet A_{panel} \ \ W/m^2 \ ,$$

which means that a PV panel or array would produce 844 W per kW rated power.
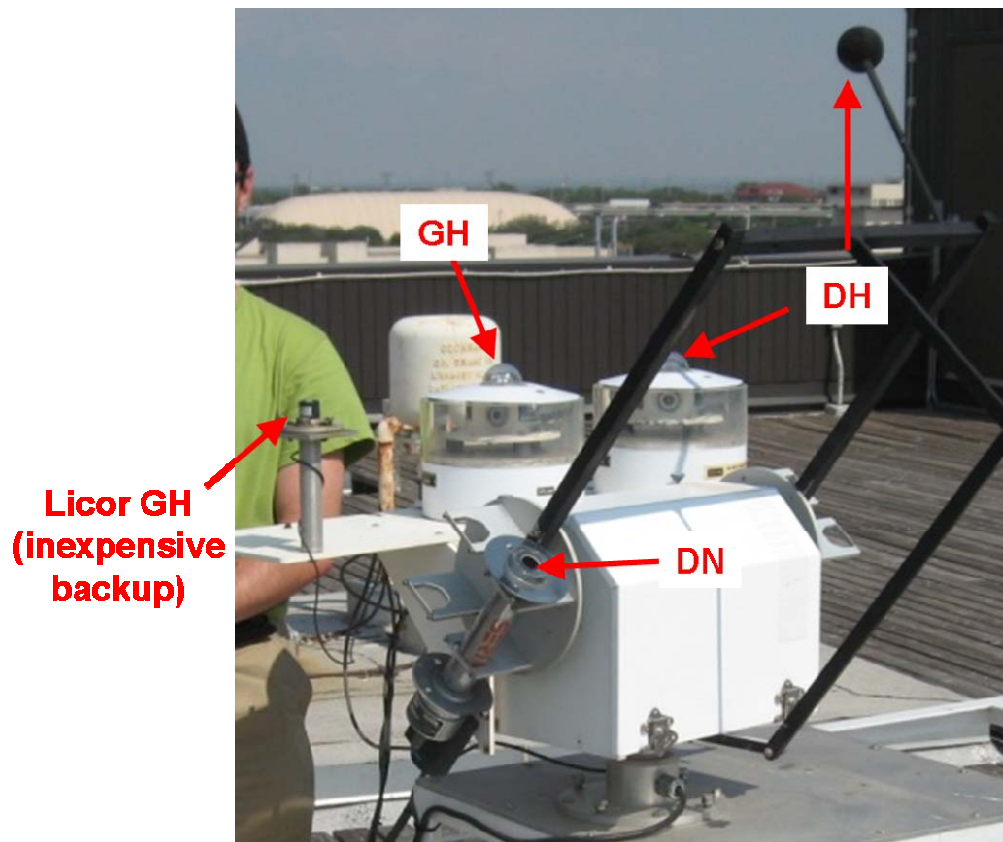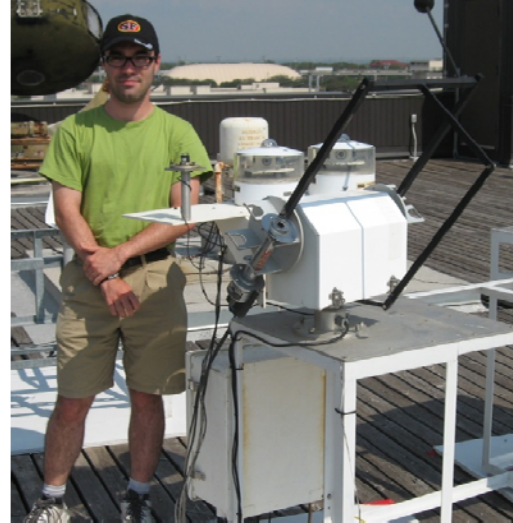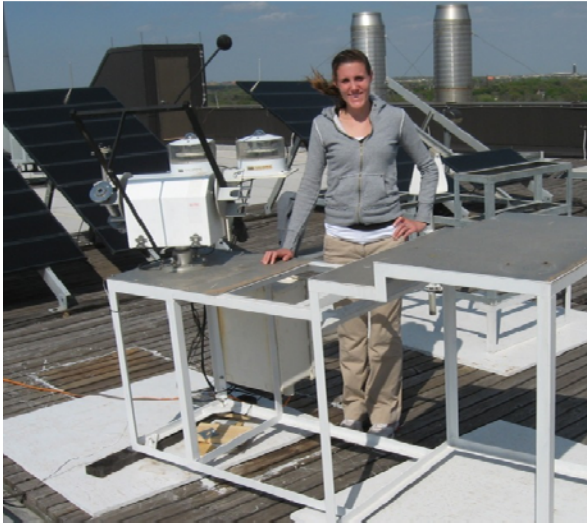
NREL Sci Tec Two-Axis Tracker

The Experiment
Your assignment is to measure the I-V and P-V characteristics of a solar panel pair, plot the points, determine maximum power, estimate panel efficiency, and use the Excel Solver to approximate the I-V and P-V curves using

$$I = I_{sc} - A(e^{BV} - 1) , \ P = VI = V \bullet \left[I_{sc} - A(e^{BV} - 1) \right],$$

where the Solver estimates coefficients I_{sc}, A, and B from your measured I-V data set. See the Appendix for a description of the Excel Solver.

Experimental Procedure
You will need about 30 minutes to take the experimental data. Go to an available panel station, and check the short circuit current. Take your measurements when the short circuit current is at least 3.5A (try for a sunny day, between 11am and 3pm.). (Note - weather site www.weatherunderground.com can help you make your plans for upcoming days.) Then, using the voltage **at the panel (i.e., the left-most meter in the yellow solar panel interface box)**, and the panel ammeter (the right-most meter), perform the following steps given below, **recording and plotting your data on the experimental form and on the graph as you go**:

| **Voltage at solar panel** | Voltage at lab bench (don't record) | **Current** |

EE462L, Power Electronics, Solar Power, I-V Characteristics
Version September 13, 2010

Form and Graph for Recording and Plotting Your Readings as You Take Them
(have this page signed by Dr. Grady before beginning your report)

Panel Station = _____ Date and Time of Measurements= _____, Sky Conditions = _____

V_{panel}*	I_{panel}*	P (i.e., $V_{panel} \bullet I_{panel}$)	Notes
V_{oc} =			Open circuit condition
	I_{sc} =		Short Circuit Condition

≈2V spacing for V > 25V

≈5V spacing for V ≤ 25V

* V_{panel} (**i.e., at the panel**) is the left-most meter in the yellow interface box, and I_{panel} is the right-most meter.
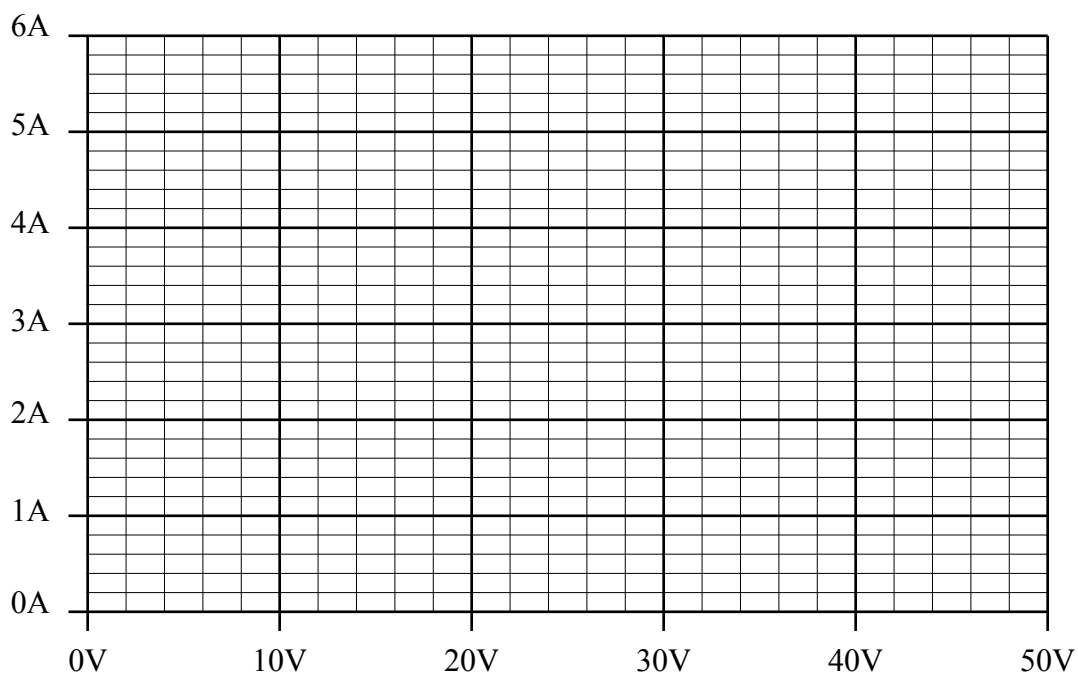
Steps

1. Measure the panel pair's open circuit voltage, and record in the table and on the graph. The current is zero for this case.
2. Short the output terminals with one of the red shorting bar or with a wire. Measure the short circuit current and panel pair voltage. Record both and add the point to your graph. The panel voltage will be small for this condition.
3. Connect one of the "solar testers" (i.e., the heavy-duty variable resistor boxes with the large knobs) to the panel pair output terminals. You will use the variable rheostat and switch to sweep the entire I-V curve.

4. Beginning with the near open circuit condition, (i.e., maximum resistance), lower the solar tester resistance so that the panel pair voltage decreases from open circuit toward zero in steps of approximately 2V between 25-40V, and in 5V steps below 25V. Record panel pair voltage and current at each step, and hand plot I versus V results as you go. If your points do not form a smooth curve, you may want to retake the outliers. Cloud movement can cause these variations.

The laboratory measurement portion of the experiment is now completed. Your graph should be fairly smooth and free of outlying points. You can now leave the lab bench.

Next, you will

5. Download Excel file EE362L_PV_Plots_Solver.xls from the course web page, and then enter your V and I values in Excel. Modify the plot command so that all the data for your experiment will be plotted. Plot I versus V points, and $P = V \cdot I$ versus V points **using the "scatter plot" option**.
6. Visually estimate V_m, I_m, and P_{max} (i.e., peak power conditions) from your plots.

7. Use the Excel Solver to compute coefficients I_{sc}, A, and B from your I-V data. Modify the Solver command so that all your data will be included in the calculations.

Superimpose the Solver equations on the I-V and P-V graphs of Step 5. See the Appendix for Solver instructions. Use your Solver graph to estimate P$_{max}$.

Now, use the following steps to estimate panel pair efficiency:

8.   Go to the class web page and download the Excel spreadsheet and solar data file

        EE362L_Solar_Data_Analyzer.xls, and

        UTAUSTIN_SHADOW_BAND.dat..

        Note – the 5-minute data averages are recorded by a shadow band tracker atop ETC and are updated daily on the web page while EE362L is being taught.

9.   Display the data for your day (note – these data are given in Central Standard Time).

10.   Using the program options, graphs, and columns, view the following for the time of your measurements:
- Direct normal, global horizontal, and diffuse horizontal power densities
- Sun azimuth and zenith angles
- $\cos(\beta_{incident})$
- Incident power on panel

11.   Use Equation (15) to estimate the incident panel power density (Watts per square meter). Compare your result to the spreadsheet value. Divide your measured maximum power by the estimated incident panel power to determine panel efficiency.

Appendix A: Using the Excel Solver to Curve-Fit Measured Data
The Excel Solver is not part of the "Typical User" installation. Check to see if the Solver is activated in your Excel installation by selecting "Tools," and then "Add-Ins." If Solver is checked, it is ready for use. Otherwise, check "Solver Add-In," and Excel will guide you through the steps. It will probably be necessary to insert your Excel installation CD rom.
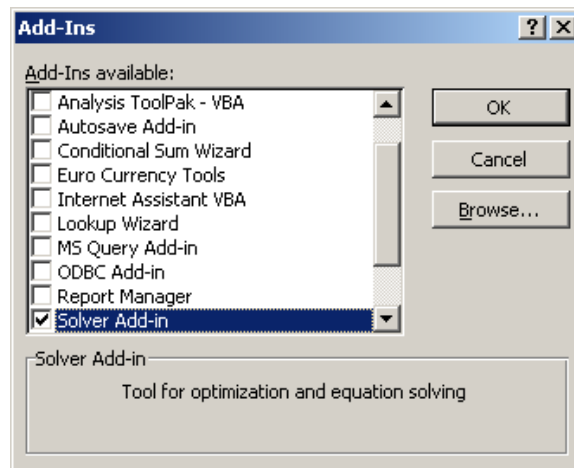
To use Solver, refer to the following page. Enter your V and I data, and establish cells for I equation coefficients Isc, A, and B. Then, key-in the I equation shown previously to form a

column of predicted currents, linking each cell to the Isc, A, and B cells. Next, establish a
column of squared errors for current, and then one cell with sum of squared errors.

Coefficients of I Equation

PV Station 13			Isc=	5.340E+00
			A=	5.232E-03
			B=	1.778E-01

	Vpanel	I	I equation	(I error)^2	Ppanel = VI
	39	0	-1.837E-02	0.000337	0.0
	35	2.65	2.711E+00	0.003701	92.8
	30	4.3	4.262E+00	0.001448	129.0
	25	4.95	4.900E+00	0.002531	123.8
	20	5.15	5.162E+00	0.000142	103.0
	4	5.3	5.334E+00	0.001179	21.2
				0.009338	

Add rows so you can enter all your data points

Currents Predicted by I Equation

Sum of Squared Errors

Individual Squared Errors

Now, under "Tools," select "Solver." The following window will appear. Enter your "Target
Cell" (the sum of squared errors cell), plus the "Changing Cells" that correspond to Isc, A, and
B. **It is for your starting values for I_{SC}, A, and B are reasonable. You should probably use
the A and B values shown above as your starting point. Use your own measured short
circuit current for I_{SC}.**

Solver Parameters

Set Target Cell: $E$11

Equal To: ○ Max ◉ Min ○ Value of: 0

By Changing Cells:

$F$1:$F$3   Guess

Subject to the Constraints:

Add
Change
Delete

Solve
Close
Options
Reset All
Help
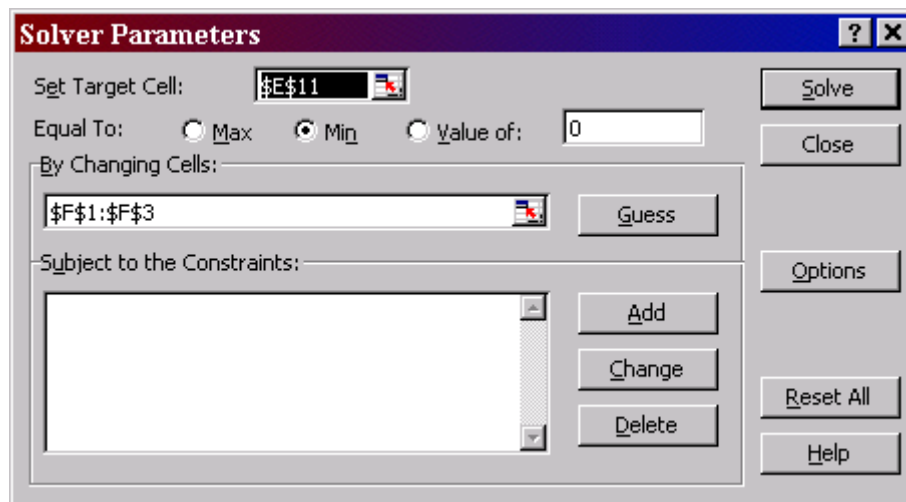
Be sure to request "Min" to minimize the error, and then click "Solve."
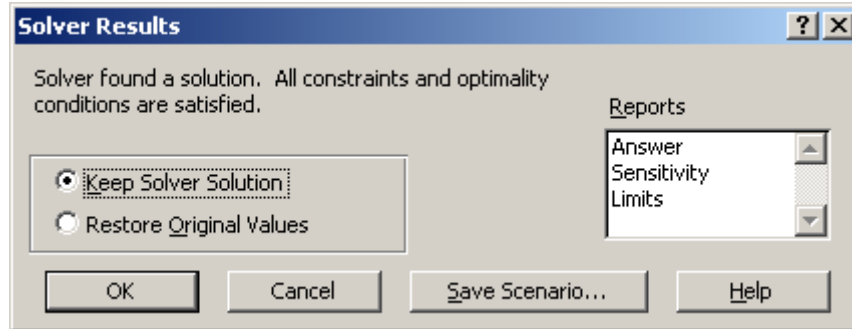
If successful, click "OK" and then plot your measured I, and your estimated I, versus V to make a visual comparison between the measured and estimated currents. Use the scatter plot option to maintain proper spacing between voltage points on the x-axis.

If unsuccessful when curve fitting, try changing I_{SC}, A, or B, and re-try.

Appendix B: National and State Solar Insolation Data

Direct Solar Insolation Levels

(courtesy of Texas State Energy Conservation Office, www.infinitepower.org)

Desert regions of Far West Texas contain the suniest areas in the state as well as some of the suniest in the nation.

In general, sunshine increases rather uniformly with distance from the Gulf Coast

This map is based on measurements at only five (5) locations in Texas. Particularly in the mountainous Trans-Pecos and in the Rio Grande Valley, solar patterns are more complex than indicated here. For instance, Laredo and Big Bend probably receive more sunshine then indicated.

AVERAGE DIRECT NORMAL INSOLATION MAP LEGEND			
COLOR KEY	per day (kWh/m²-day)	per YEAR	
		(MJ/m2)	(quads/100 mi²)
	<3.0	<3,940	<1.0
	3.0 - 3.5	3,940 - 4,600	1.0 - 1.1
	3.5 - 4.0	4,600 - 5,260	1.1 - 1.3
	4.0 - 4.5	5,260 - 5,910	1.3 - 1.5
	4.5 - 5.0	5,910 - 6,570	1.5 - 1.6
	5.0 - 5.5	6,570 - 7,230	1.6 - 1.8
	5.5 - 6.0	7,230 - 7,880	1.8 - 1.9
	6.0 - 6.5	7,880 - 8,540	1.9 - 2.1
	6.5 - 7.0	8,540 - 9,200	2.1 - 2.3
	>7.0	>9,200	>2.3

Solar Data Analyzer, Prof. Mack Grady, U.T. Austin, Sept. 17, 2009.

STEP 1. Read Solar Radiation Data

Path
C:\SOLAR_DATA\

☐ Proceed Without Logger Data

File Names (5 minute data only)
- ○ UTAUSTIN_NREL.dat
- ● UTAUSTIN_SHADOW_BAND.dat
- ○ SARAGOSA.dat
- ○ UT_EL_PASO_NREL.dat

File Name
UTAUSTIN_SHADOW_BAND.dat

READ DATA FILE   OK

Single Day Analysis

Year	Day of Year	Mon/Day
2009	264	Sep. 21

Clear Sky, kWh/m2
7.19

Method 1, kWh/m2
6.93

Method 2, kWh/m2
1.86

Licor_PA, kWh/m2
0.00

Multiple Day Analysis

RUN MULTIPLE

Number of Days
10

Clear Sky, kWh/m2
0

Method 1, kWh/m2
0

Method 2, kWh/m2
0

Licor_PA, kWh/m2
0

Notes – Only the bold PUSH BUTTONS and the DAY SLIDEBAR invoke action. Once invoked, the program reads the information and passes it to the spreadsheet for calculations. When finished, use the STOP PROGRAM button so that the files are properly closed.

Parameters

Latitude	Longitude Shift	Extraterrestrial Solar Radiation
30.29	-7.74	1377

Panel Tilt	Panel Azimuth	Reflected Coef.
45	190	0.2

RESTORE DEFAULTS

Sweep Panel Angles for Multiple Days Selected Above

SWEEP

Tilt Start	Tilt Stop	Tilt Stepsize - Deg
0	60	● 5 ○ 10 ○ 15

Azimuth Start	Azimuth Stop	Azimuth Stepsize - Deg
90	270	○ 5 ● 10 ○ 30

Output File Options

Name Extension

☐ Use Date/Time Extension

Tracking
- ● None
- ○ Single-Axis Rotation, Tilt and Az Specified
- ○ Tilt Tracking, Az Specified
- ○ Sun Following

First Two Lines Read from Solar Radiation Data File
128,4,2009,217,620,48.83,0,37.13,0,0
128,4,2009,217,625,65.39,0,43.79,0,0

Last Two Lines Read from Solar Radiation Data File
128,4,2009,267,1025,176.3,0,174.7,0,0
128,4,2009,267,1030,210.4,0,209.1,0,0

Errors

STOP PROGRAM

Spreadsheet cells:

	A	B	C	D	E	F	G	H	I	J	K	L	M	N
1	EXECUTE	1. For faster sweep execution, minimize the screen hide the graphs.						5 minute data only	Tracking Method		Clear Sky kWH/m2	Calc. Method 1 kWH/m2	Calc. Method 2 kWH/m2	Licor kW
2		2. Is best to not re-save this spreadsheet in case you have accidently							0 = None					
3	Year	changed some of the cells that contain imbedded instructions or formulas.							1 = Single Axis		One Day	One Day	One Day	One
4	2009	3. Graphs 1 and 2 are updated through the user interface screen.							2 = Tilt Only		7.19	6.93	1.86	0
5	Day of Year	Measurement and Panel Latitude	Measurement and Panel Longitude Shift			Panel Tilt	Panel Az.	Daily Sun Hours	3 = Sun Following		Sum of Days	Sum of Days	Sum of Days	Sum
6	264	30.29	-7.74			45	190		0		0.00	0.00	0.00	0

Solar Measurements, File UTAUSTIN_SHADOW_BAND.dat
(GH, DN, DH, Licor_PA, Licor_GH)
W/m2
Year 2009, Day 264, Sep. 21

21	0	40	0.667	0.266	176.013
22	0	45	0.750	0.349	174.763
23	0	50	0.833	0.432	173.513
24	0	55	0.917	0.516	172.263

Sun Zenith Angle - Degrees from Vertical
Degrees
Day 264, Sep. 21, Lat. 30.29, Long. Shift -7.74

41	2	20	2.333	1.932	151.013
42	2	25	2.417	2.016	149.763
43	2	30	2.500	2.099	148.513

Solar Time wrt Clock Time, Lat. 30.29, Long. Shift -7.74
Minutes
Day of Year

Sun Zenith Angle (Vertical) vs. Azimuth Angle (Horizontal)
Zenith Angle - Degrees
Day 264, Sep. 21, Lat. 30.29, Long. Shift -7.74

EE462L, Fall 2010
MOSFET Firing Circuit

1

Power MOSFETs
(high-speed, voltage-controlled switches that allow us to operate above the 20kHz audible range)

D: Drain

G: Gate

S: Source

D

G

S

If desired, a series blocking diode can be inserted here to prevent reverse current

Switch closes when $V_{GS} \approx 4V$, and opens when $V_{GS} = 0V$
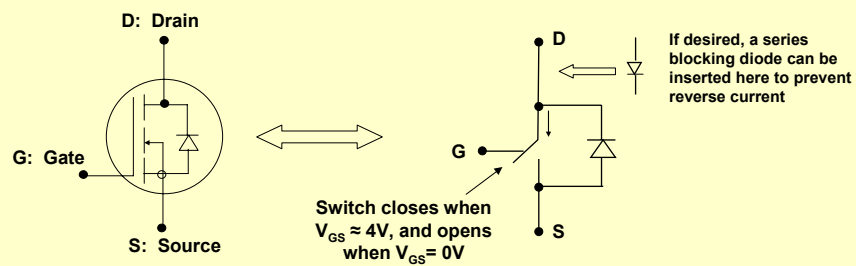
N channel MOSFET equivalent circuit

Controlled turn on, controlled turn off

(but there is an internal antiparallel diode)

2

We Avoid the Linear (Lossy) Region, Using Only the On and Off States

MOSFET "on"

D

S
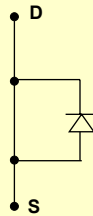
when V_{GS} = 12V

MOSFET "off"

D

S
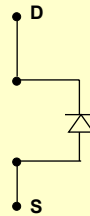
when V_{GS} = 0V

3

We Want to Switch Quickly to Minimize Switching Losses

Turn Off

$V_{DS}(t)$

0

$I(t)$

Δt_{off}

0

$P_{LOSS}(t)$

Energy lost per turn off

0

Turn On

$V_{DS}(t)$

0

$I(t)$

Δt_{on}

0

$P_{LOSS}(t)$

Energy lost per turn on

0
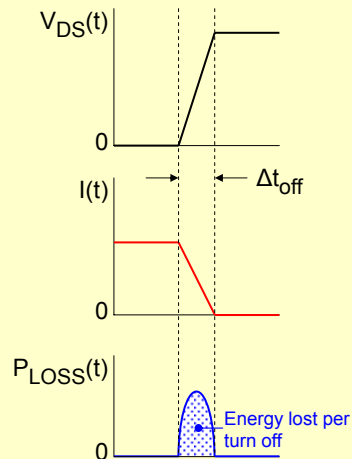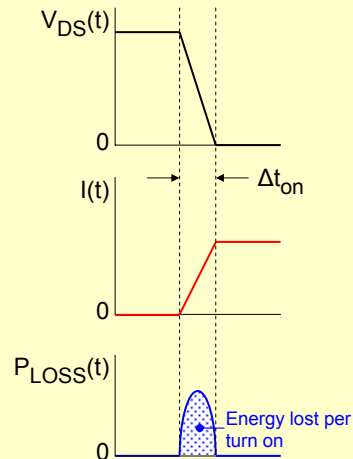
Turn off and turn on times limit the frequency of operation because their sum must be considerably less than period T (i.e., 1/f)

4

Consider, for example, the turn off

Turn Off

$V_{DS}(t)$

V

0

$I(t)$

I

0

$P_{LOSS}(t)$

Δt_{off}

Energy lost per turn off

0
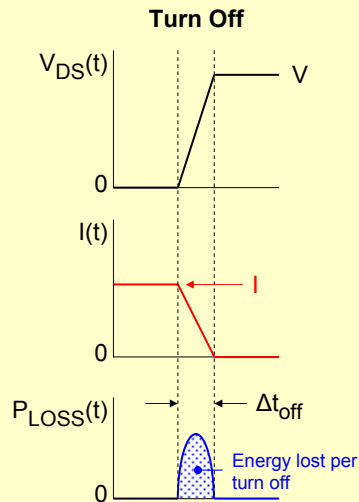
Energy lost per turn off is proportional to

$$V \bullet I \bullet \Delta t_{off} ,$$

so we want to keep turn off (and turn on) times as small as possible.

The more often we switch, the more "energy loss areas" we experience per second.

Thus, switching losses (average W) are proportional to switching frequency f, V, I, Δt_{off}, and Δt_{on}.

And, of course, there are conduction losses that are proportional to squared I

5

Advantages of Operating Above 20kHz

Yes, switching losses in power electronic switches do increase with operating frequency, but going beyond 20kHz has important advantages. Among these are

• **Humans cannot hear the circuits**

• **For the same desired smoothing effect, L's and C's can be smaller because, as frequency increases and period T decreases, L's and C's charge and discharge less energy per cycle of operation. Smaller L's and C's permit smaller, lighter circuits.**

• **Correspondingly, L and C rms ripple currents decrease, so current ratings can be lower. Thus, smaller, lighter circuits.**

• **AC transformers are smaller because, for a given voltage rating, the peak flux density in the core is reduced (which means transformer cores can have smaller cross sectional areas A).**

$$v(t) = N \frac{d\Phi}{dt} = NA \frac{dB}{dt} = NA \frac{d\left(B_{\max}\sin(\omega t)\right)}{dt} = NA B_{\max} \omega \cos(\omega t)$$

Thus, smaller, lighter circuits.

6

MC34060A, MC33060A

Fixed Frequency, PWM, Voltage Mode Single Ended Controllers

The MC34060A is a low cost fixed frequency, pulse width modulation control circuit designed primarily for single–ended SWITCHMODE™ power supply control.

The MC34060A is specified over the commercial operating temperature range of 0° to +70°C, and the MC33060A is specified over an automotive temperature range of –40° to +85°C.

- Complete Pulse Width Modulation Control Circuitry
- On–Chip Oscillator with Master or Slave Operation
- On–Chip Error Amplifiers
- On–Chip 5.0 V Reference, 1.5% Accuracy
- Adjustable Dead–Time Control
- Uncommitted Output Transistor Rated to 200 mA Source or Sink
- Undervoltage Lockout

ON Semiconductor™

http://onsemi.com

MARKING DIAGRAMS

SO–14
D SUFFIX
CASE 751A

MC3x060AD
AWLYWW

PDIP–14
P SUFFIX
CASE 646

MC3x060AP
AWLYYYWW
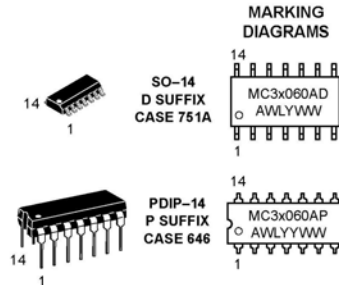
7

Description

The MC34060A is a fixed–frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply (see Figure 1). An internal–linear sawtooth oscillator is frequency–programmable by two external components, R_T and C_T. The approximate oscillator frequency is determined by:

$$f_{osc} \cong \frac{1.2}{R_T \cdot C_T}$$

Keep in mind that your C_T may be 20% higher than labeled
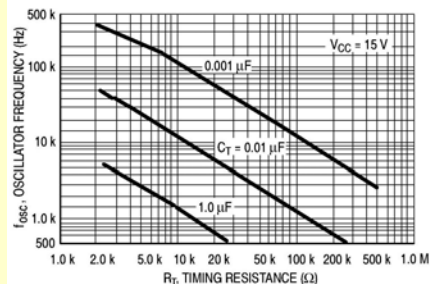
Figure 3. Oscillator Frequency versus Timing Resistance
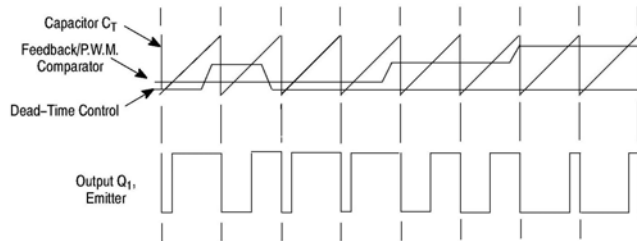
Figure 2. Timing Diagram

8

MOSFET Firing Circuit
Prof. Mack Grady, 9/16/10

S D
Gate
100k
Red 2.2k
100k
Driver
GND
PWM
Ext Man
33k
SPDT
10uF
Freq. Cont. Resistor
0.01 uF 6.8 nF
1k 4.7k
10uF
+ 12V −
1k
Orange
External Duty Input
B10k Manual Duty

9

$$f_{osc} \cong \frac{1.2}{R_T \bullet C_T}$$

Noninv Input 14	Inv Input 13	V_{ref} 12	N.C. 11	V_{CC} 10	C 9	E 8

Error 2 Amp
5.0 V ref
V_{CC}
Error Amp
0.1V
Oscillator
Q1

Noninv Input 1	Inv Input 2	Compen/PWM Comp Input 3	Dead-Time Control 4	C_T 5	R_T 6	Ground 7

10

MOSFET Gate Driver – Assures Rapid Turn On and Off

TC1426CPA

Pin	
1	NC
2	IN A
3	GND
4	IN B
8	NC
7	OUT A
6	V_DD
5	OUT B

2, 4 → 7, 5 Inverting
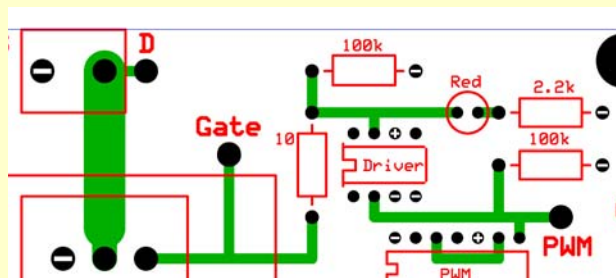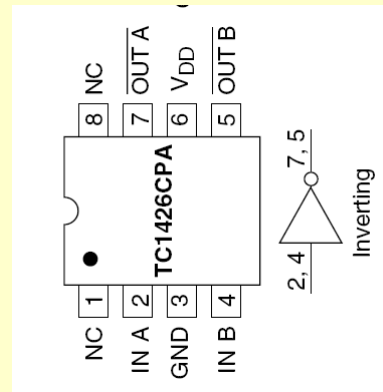
11

To control the duty cycle and provide fast turn-on and turn-off, we use

- **A 0-12V signal from a MOSFET driver chip to very quickly turn the MOSFET on and off at 20kHz-100kHz by charging and discharging the MOSFET gate capacitance (nano Farads)**

- **A pulse-width modulator (PWM) chip to provide a 0-5V control input to the MOSFET driver chip**

- **A 0-3.5V analog voltage to control the duty cycle of the PWM chip**

12

The PWM chip has an internal sawtooth wave generator, whose frequency is controlled by an external R and C

Internal sawtooth

3.5V

0-3.5V adjustable analog input

Output of PWM chip

5V

Comparison yields 0-5V control input to driver chip

Output of inverting driver chip goes to MOSFET gate

12V
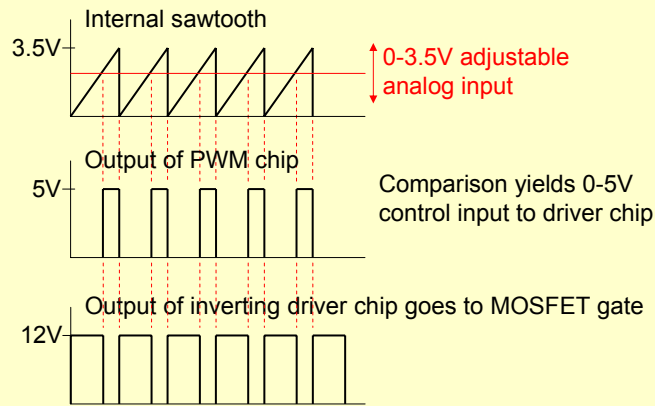
So, raising the 0-3.5V analog input raises the duty cycle of the MOSFET 12V gate signal

13

D vs. Potentiometer Angle

— Audio Pot
- - - Linear Pot

Potentiometer Angle

Boost Vout/Vin vs. Potentiometer Angle

Less steep at high voltages →

— Audio Pot
- - - Linear Pot
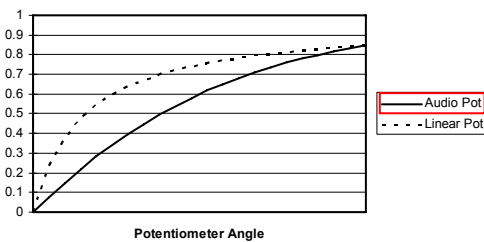
Potentiometer Angle

Buck/Boost Vout/Vin vs. Potentiometer Angle

— Audio Pot
- - - Linear Pot
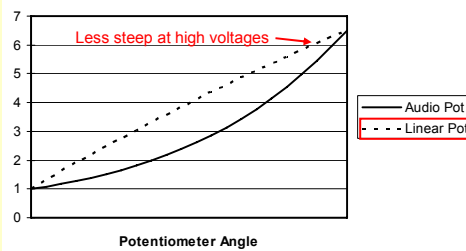
Potentiometer Angle
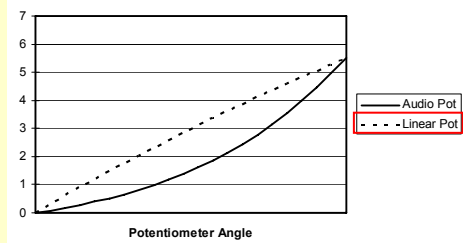
Construction Tips

- **Use #8 nylon half-inch threaded spacers as feet, with #8 nylon screws on top**

- **All soldering is done on the bottom side of the PCB**

- **Double-socket the chips – one socket stays attached to the chip for re-use each semester. The other socket is soldered to the PCB.**

- **Solder the shortest components first, and the tallest components last**

- **The soldering iron tip should be held firmly on the solder pad, and slightly touching the component**

- **Use wood props to hold components flat on the top surface while you solder the bottom side**
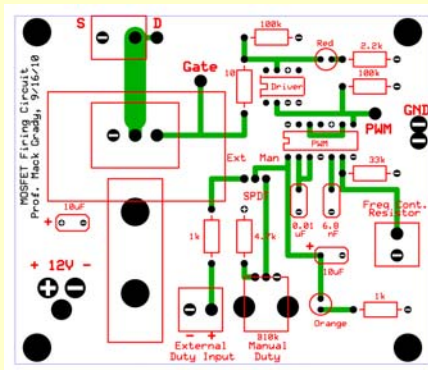
- **Traces are rated 4A per 0.1" of width. The thin ones here are 0.05", and the wide one is 0.20".**

- **It is time to memorize the color code. Ask around for a jingle.**

15

Construction Tips, cont.

- Orient the resistors so the color code reads left to right, or top to bottom

- **BEFORE SOLDERING, make sure that the green plugs point in the desired direction**

- **The long lead on LEDs is +**

- **Do not solder the MOSFET – it will be screwed to a green plug**

-

-

-

16

8

MOSFETS are Very Static Sensitive

- Touching the gate lead before the MOSFET is properly mounted with a 100kΩ gate-to-source resistor will likely ruin the MOSFET

- But it may not fail right away. Instead, the failure may be gradual. Your circuit will work, but not correctly. Performance gradually deteriorates.

- When that happens, you can spend unnecessary hours debugging

- Key indicators of a failed MOSFET are

  - Failed or burning hot driver chip
  - Burning hot gate driver resistor (discolored, or bubbled up)
  - Board scorches or melts underneath the driver chip or gate driver resistor

Avoid these problems by mounting the MOSFET last, by using an antistatic wristband, and by not touching the gate lead

17

The 100kΩ gate-to-source resistor is soldered onto the PCB.

A 3-pin header strip (under the green plug) is soldered to the PCB, with the black plastic strip of the header on top of the PCB.

Before taking the MOSFET out of the pink zip bag, push the green plug down (hard) onto the header strip.

Then, using an antistatic wristband, and without touching the gate lead, insert the MOSFET into the green plug and tighten the three screws.

After that, mount the heat sink assembly with nylon hardware and tighten the MOSFET firmly to the heat sink.

G: Gate   D: Drain   S: Source
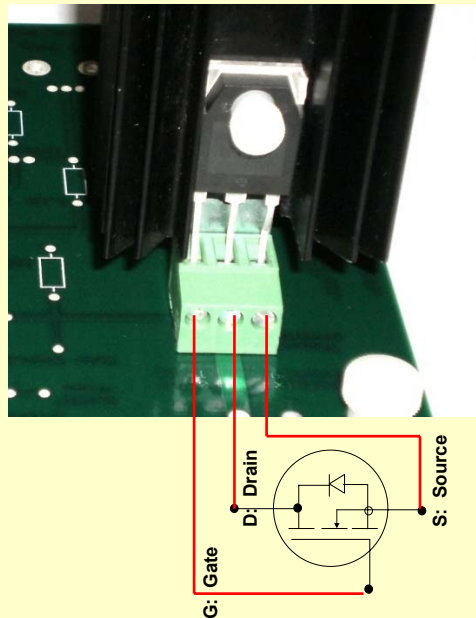
18

No-Load Tests

Take simultaneously screen snapshots of PWM output AND

Freq(1): 50.57kHz
Pk-Pk(1): 4.53V
Duty(1): 20.4%

Print to disk file: PRINT_02
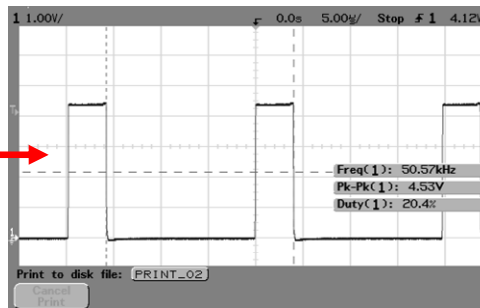
PWM Logic Output (i.e., Pin 8)

VGS for 100 kHz. Repeat for 200 kHz. Plus or minus 10-15% freq is OK.

Expect clean, sharp rectangular waveforms at 100 kHz, and some rounding of corners at 200 kHz.

Freq(1): 50.44kHz   Pk-Pk(1): 11.69V   Duty(1): 80.2%
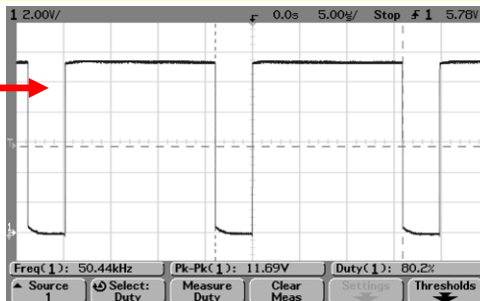
Open-Circuited Driver Chip Output V$_{GS}$

19

Hard Switching Load Tests (i.e., full interruption of load current with parasitic line inductance). Start with 100kHz.

- **Before turning on the variac/rransformer/DBR, connect scope leads to simultaneously view VGS and VDS.**

- **Set the D control to zero. Raise Vdc (i.e., the DBR voltage) to about 20V.**

- **While viewing VGS and VDS, slowly raise D to about 0.5. Observe and measure the peak value and frequency of the ringing overvoltage in VDS.**

- **Sweep D over the entire range. Does the ringing overvoltage increase with D?**

- **If no sign of trouble, repeat the above with the Vdc about 35 to 40V. Take a screen snapshot of VDS. Measure the peak value and frequency of the ringing overvoltage.**

- **If no sign of trouble, repeat with 200kHz.**

Variac → 120/25V Transformer → DBR (+ −)

10Ω, 100W power resistor

If peak ringing overvoltage reaches 200V, back off on Vdc
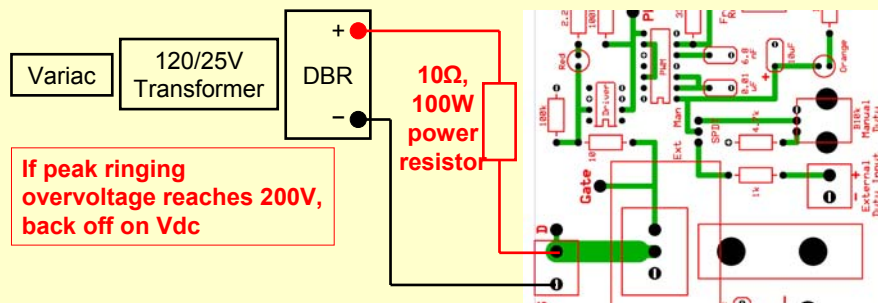
Controlling the Ringing Overvoltage

- Ringing overvoltage is due to the MOSFET capacitance in series with the load circuit's parasitic inductance (including DBR, wires, and resistor)

- Obviously, in the "hard switching" case, the ringing overvoltage can be greater than the acceptable "twice Vdc."

- High ringing overvoltage "uses up" the MOSFET's voltage rating

- To reduce ringing overvoltage, "slow it down" by placing a 0.022 μF ceramic disk capacitor (a.k,a "snubber capacitor") between the MOSFET's drain and source terminals.

- Then, repeat the hard switching load test with 35-40 Vdc, D = 0.5, and re-measure the frequency and peak value of the ringing overvoltage.

21

Large 10Ω , 225W Resistor. 5.3Vdc. Vpeak = 200V.

22
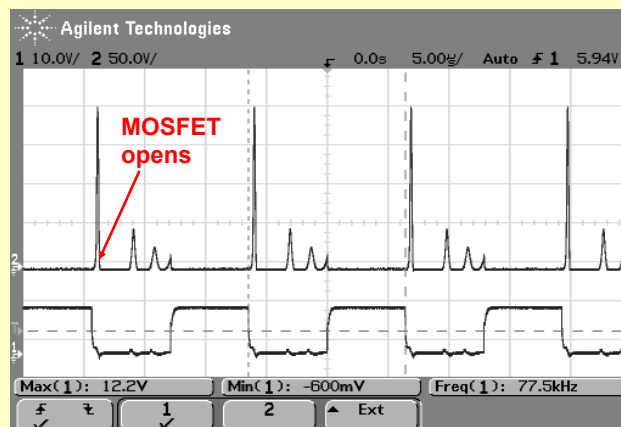
Small 10Ω , 100W Resistor. 22Vdc. Vpeak = 240V.
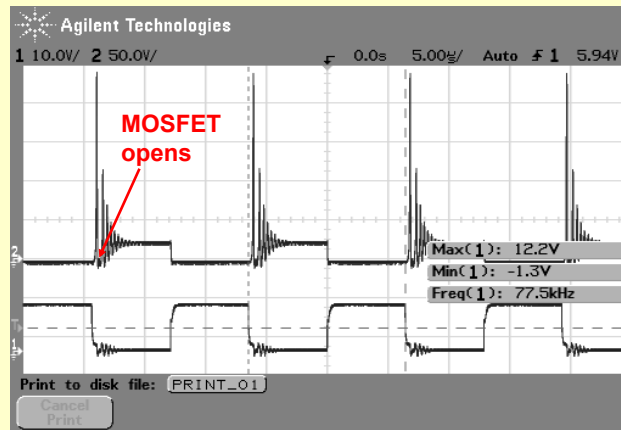
Small 10Ω , 100W Resistor. 20Vdc. Vpeak = 240V.
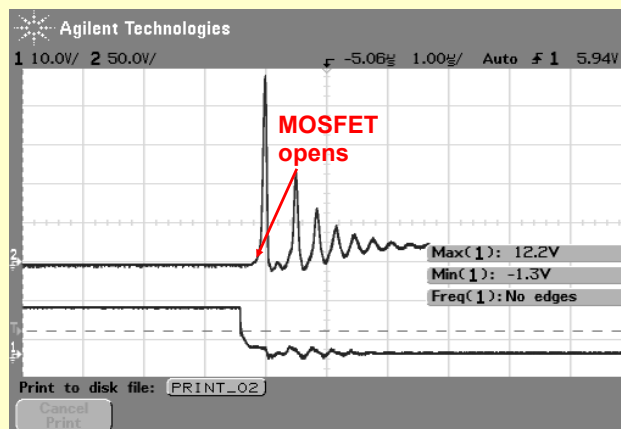
Small 10Ω , 100W Resistor. 22Vdc. Vpeak = 40V.

0.022µF Snubber Cap

25
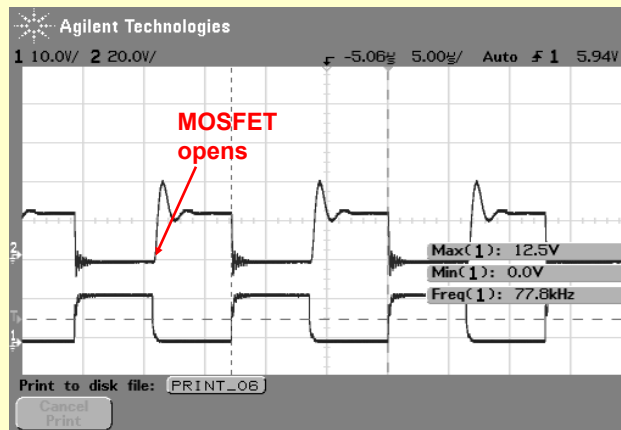
Small 10Ω , 100W Resistor. 22Vdc. Vpeak = 60V

0.0068µF Snubber Cap

26

EE462L, Power Electronics, DC-DC Buck Converter
Version Oct. 4, 2010
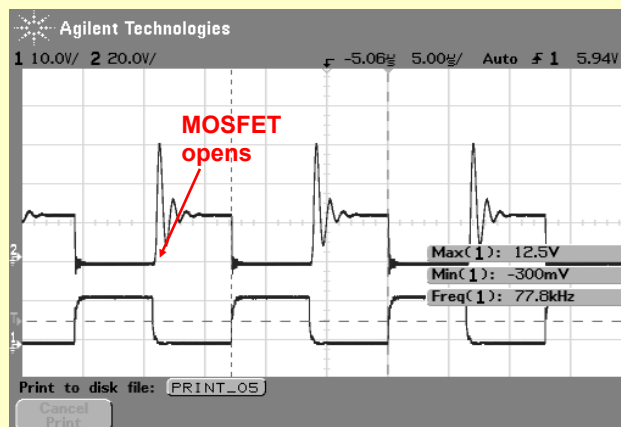
Overview
DC-DC converters provide efficient conversion of DC voltage from one level to another. Specifically, the term "buck" converter means that the converter takes input from a higher voltage level, e.g. variable 36-42V from solar panels, and converts it to a lower voltage level, e.g. fixed 12V, for powering equipment.

Theory of Operation

Relation Between V_{out} and V_{in} in Continuous Conduction

The idealized buck converter circuit is shown below in Figure 1. Input voltage V_{in} is assumed to be ripple free. The power electronic switch opens and closes at a fixed rate of, for example, 100kHz, and its duty cycle is varied to control V_{out}. Capacitor C is assumed to be large enough so that V_{out} has a ripple of less than 5% and is therefore, essentially ripple free. I_{out} is also assumed to be ripple free. In normal operation, the circuit is in "continuous conduction," e.g. i_L is always greater than zero.
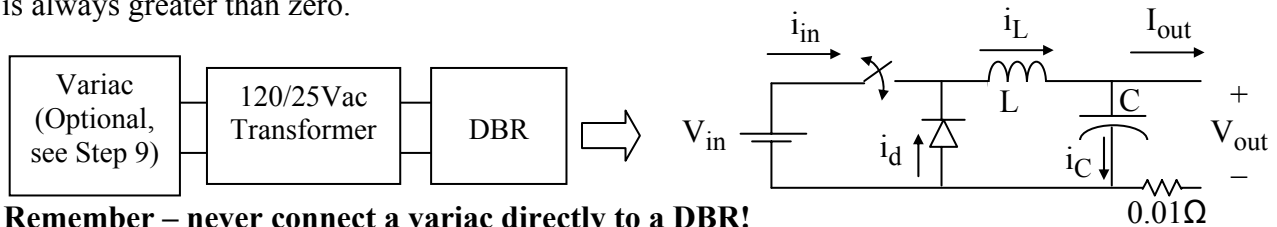
Remember – never connect a variac directly to a DBR!

Figure 1. DC-DC Buck Converter
(note - you will mount a 0.01Ω resistor at the negative V_{out} terminal to measure output current, and a 10μF ripple current capacitor across the V_{in} terminals to reduce overshoot caused by lead inductance)

The circuit is assumed to be lossless so that $P_{in} = P_{out}$, so

$$V_{in} \bullet i_{inavg} = V_{out} \bullet I_{out} \ . \tag{1}$$

Assuming continuous conduction, the circuit has two topologies – switch closed, and switch open. These are shown in Figures 2a and 2b.
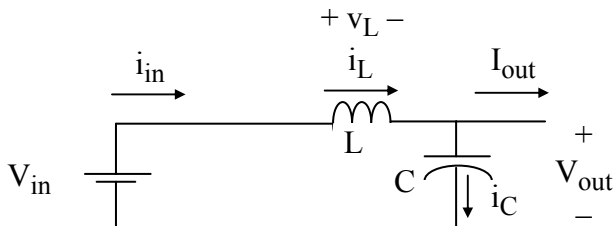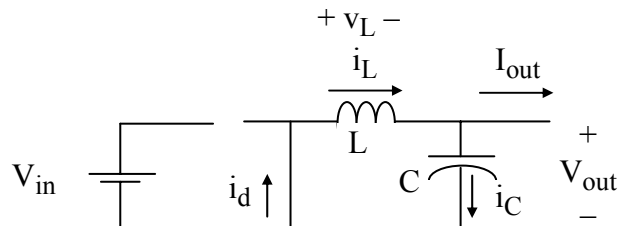
Figure 2a. Switch Closed for DT Seconds

Figure 2b. Switch Open for (1-D)T Seconds (Continuous Conduction)

When the switch is closed, the diode is reverse biased and open, and i_L increases at the rate of

$$\frac{di_L}{dt} = \frac{v_L}{L} = \frac{V_{in} - V_{out}}{L}, \ 0 \le t \le DT, \tag{2}$$

and the inductor is "charging." When the switch is open, i_L continues to circulate through the diode, the diode is forward biased, i_L decreases at the rate of

$$\frac{di_L}{dt} = \frac{v_L}{L} = \frac{-V_{out}}{L}, \ DT < t < T, \tag{3}$$

and the inductor is "discharging." The inductor voltage is shown in Figure 3.
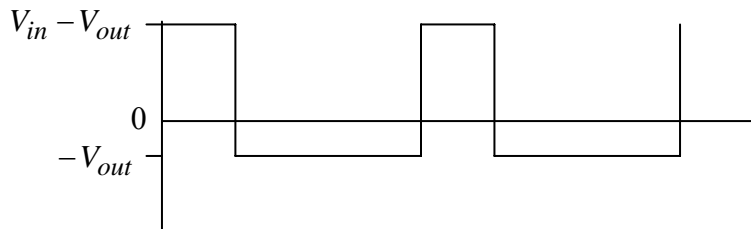
Figure 3. Inductor Voltage in Continuous Conduction

Because of the steady-state inductor principle, the average voltage v_L across L is zero. Since v_L has two states, both having constant voltage, the average value is

$$\frac{(V_{in} - V_{out})DT + (-V_{out})(1 - D)T}{T} = 0, \ \text{so that}$$

$$V_{in}D - V_{out}D - V_{out} + V_{out}D = 0 \ .$$

Simplifying the above yields the final input-output voltage expression

$$V_{out} = V_{in}D \ . \tag{4}$$

Inductor Current in Continuous Conduction

Equations (2) and (3) give the rate of rise and fall of i_L. The average value of i_L is found by examining the node at the top of capacitor C in Figure 1. Applying KCL in the average sense, and recognizing that the average current through a capacitor operating in steady state is zero, it is obvious that

$$i_{Lavg} = I_{out} \tag{5}$$

Equations (2), (3), and (5) provide the necessary information to draw a graph if i_L, as shown in Figure 4.

$$i_{L\max} = i_{Lavg} + \frac{\Delta I}{2}$$

$$i_{Lavg} = I_{out}$$
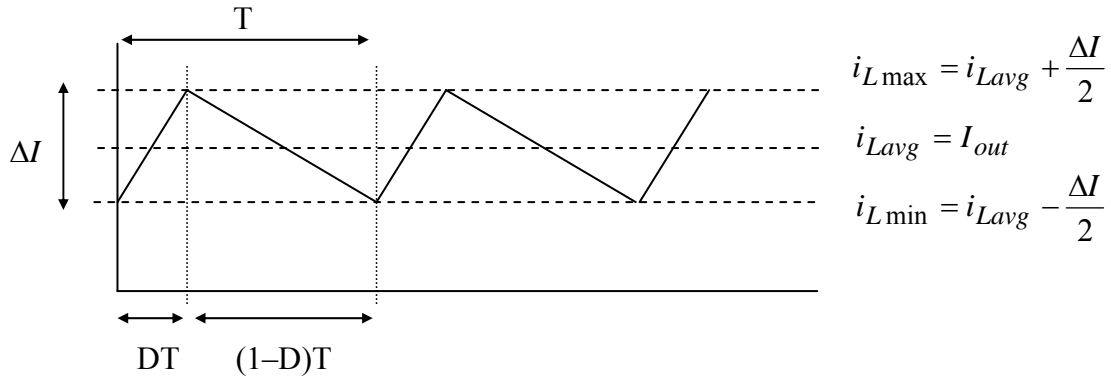
$$i_{L\min} = i_{Lavg} - \frac{\Delta I}{2}$$

Figure 4. Inductor Current Waveform for Continuous Conduction

Because the current consists of straight line segments, it is obvious that

$$i_{Lavg} = \frac{i_{L\max} + i_{L\min}}{2} \;,\; i_{L\max} = i_{Lavg} + \frac{\Delta I}{2} \;,\; i_{L\min} = i_{Lavg} - \frac{\Delta I}{2} \;.$$

From (2),

$$\frac{di_L}{dt} = \frac{V_{in} - V_{out}}{L} = \frac{\Delta I}{DT} \;,$$

so that

$$\Delta I = \frac{V_{in} - V_{out}}{L} \bullet DT = \frac{V_{in} - DV_{in}}{L} \bullet DT = \frac{V_{in}D(1-D)}{Lf} \tag{6}$$

where f is the switching frequency. Taking the derivative of (6) with respect to D and setting it to zero shows that ΔI is maximum when D = ½. Thus,

$$\Delta I_{\max} = \frac{V_{in}}{4Lf} \tag{7}$$

Through the definition of rms, it can be shown that the squared rms value of the triangular waveform in Figure 4 is

$$I_{rms}^2 = I_{avg}^2 + \frac{1}{12}(\Delta I)^2 \;. \tag{8}$$

(Question – can you develop the above expression from the rms integral?)

The boundary of continuous conduction is when $i_{L\min} = 0$, as shown in Figure 5.
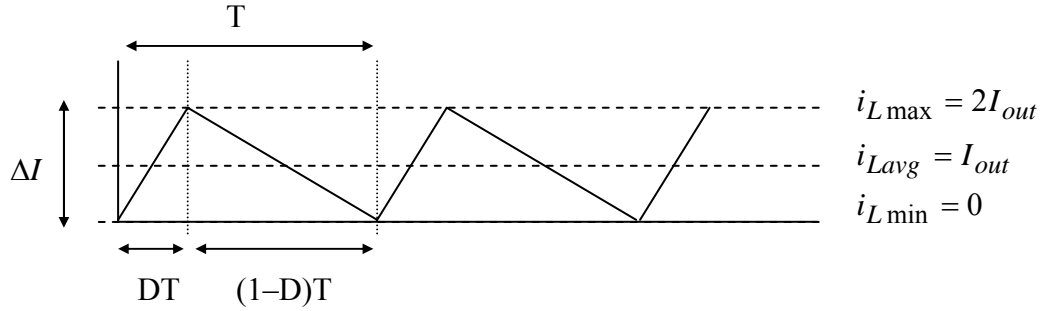
Figure 5. Inductor Current at the Boundary of Continuous Conduction

As shown, when at the boundary, $\Delta I = 2i_{Lavg} = 2I_{out}$. Using Figure 5 and the "inductor discharging" slope in (3), we get

$$\frac{-V_{out}}{L_{boundary}}(1-D)T = \frac{-V_{out}}{L_{boundary}\,f}(1-D) = -2I_{out} \, ,$$

$$L_{boundary} = \frac{V_{out}(1-D)}{2I_{out}\,f} \, , \qquad\qquad\qquad (9)$$

where $L_{boundary}$ is the value of L at the boundary of continuous conduction. The maximum $L_{boundary}$ is where $D \rightarrow 0,$ Thus

$$L > \frac{V_{out}}{2I_{out}\,f} \qquad\qquad\qquad\qquad (10)$$

will guarantee continuous conduction for all D. Note in (10) that continuous conduction can be achieved more easily when I_{out} and f are large.

Discontinuous Conduction

At low load periods, the converter may slip into the discontinuous conduction mode. Referring back to Figure 2b, this occurs when the inductor current coasts to zero. At that moment, the capacitor attempts to reverse i_L and "backfeed" the inductor, but reversal is prevented by the freewheeling diode. Thus, the freewheeling diode opens, and the circuit assumes the topology shown in Figure 6 until the switch closes again. During this third state, all load power is provided by the capacitor.

$$+ \; 0 \; -$$
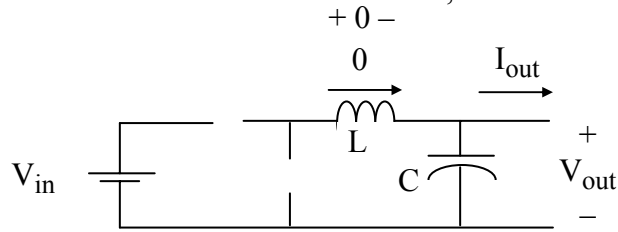
Figure 6. Third State for Discontinuous Conduction

Once discontinuous, the voltage across the inductor is zero. The corresponding voltage waveform is shown in Figure 7.
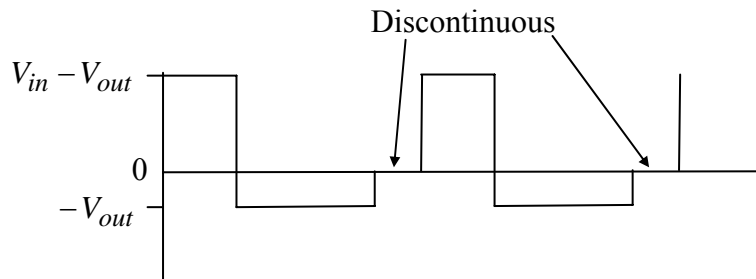
Figure 7. Inductor Voltage in Discontinuous Conduction

Capacitor Ripple Voltage in Continuous Conduction

For the node above C in Figure 1, KCL requires that

$$i_C = i_L - I_{out} \; .$$

Then, considering Figure 4, capacitor C must be charging when i_L is greater than I_{out}, and discharging when i_L is less than I_{out}, as shown in Figures 8, 9, and 10.
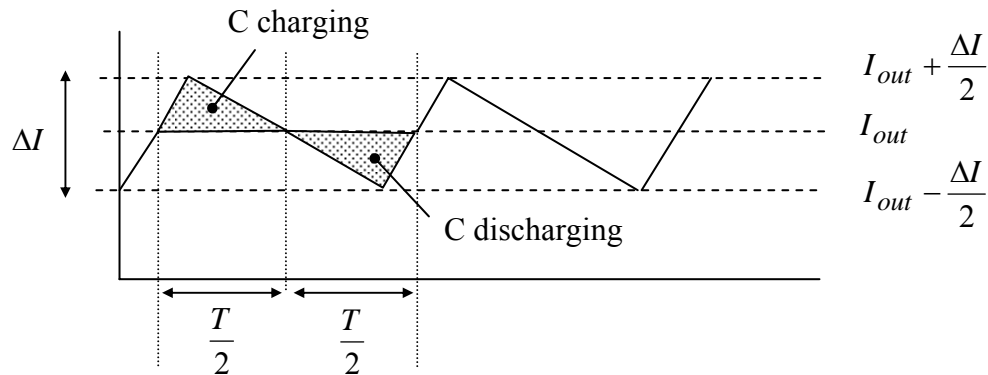
Figure 8. Inductor Current Graph Used to Illustrate Capacitor Charging and
Discharging Intervals in Continuous Conduction
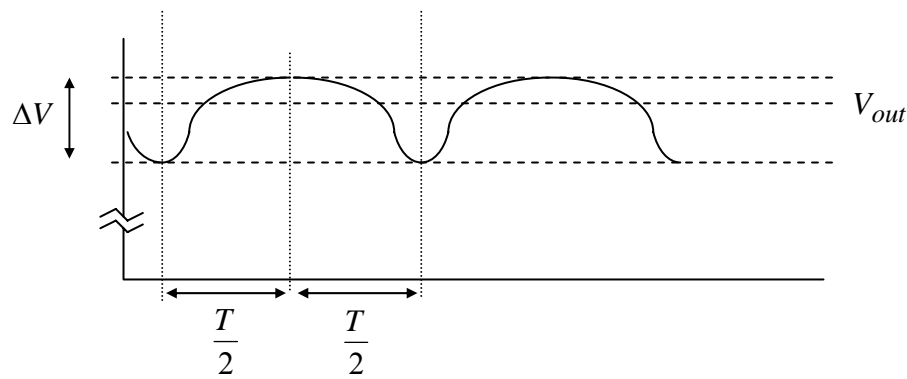
Figure 9. Capacitor Voltage in Continuous Conduction
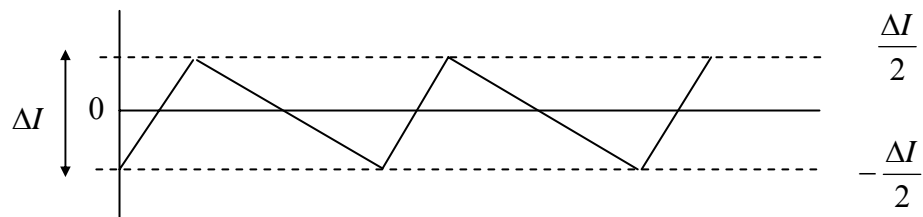
Figure 10. Capacitor Current in Continuous Conduction

Each charging and discharging area in Figure 8 lasts for $\dfrac{T}{2}$ seconds, and each area represents a charge increment ΔQ for the capacitor. The net charge flowing into the capacitor for one period must be zero in steady-state so that the capacitor voltage is periodic. Using

$$\Delta V = \frac{\Delta Q}{C} \tag{11}$$

and the area of the triangular charging region in Figure 8, the peak-to-peak ripple voltage on C must be

$$\Delta V = \frac{\Delta Q}{C} = \frac{1}{C} \bullet \frac{1}{2} \bullet \frac{T}{2} \bullet \frac{\Delta I}{2} = \frac{T\Delta I}{8C} \tag{12}$$

For the worst case, $\Delta I = 2I_{out}$, so

$$\Delta V = \frac{T}{8C} \bullet 2I_{out} \; . \tag{13}$$

Thus, the **worst case peak-to-peak voltage ripple** on C is

$$\Delta V = \frac{I_{out}}{4Cf} \; . \tag{14}$$

Component Ratings

Inductor and Capacitor Ratings – The inductor must have sufficient rms current rating for the current shown in Figure 4. The capacitor must support the maximum output voltage (i.e., corresponding to V_{in} when D = 1) and the rms ripple current shown in Figure 10. The ripple currents (i.e., total current minus average value) in Figures 4 and 10 are identical because of KCL at the node above C in Figure 1.

A conservative estimate for rms inductor current is when

$$\Delta I_{max} = 2I_{out}, \tag{15}$$

which when substituted into (8) yields

$$I_{Lrms,max}^2 = I_{out}^2 + \frac{1}{12}(2I_{out})^2 = I_{out}^2\left(1+\frac{1}{3}\right), \tag{16}$$

so that

$$I_{Lrms,max} = \frac{2}{\sqrt{3}}I_{out} \; . \tag{17}$$

The same ripple current ΔI also flows through C, but C has no average current. Using the same logic as in (15), the maximum squared rms current through C becomes

$$I_{Crms,max}^2 = 0 + \frac{1}{12}(\Delta I)^2 = \frac{1}{12}(2I_{out})^2 = \frac{I_{out}^2}{3} \; , \tag{18}$$

so that

$$I_{Crms,\max} = \frac{I_{out}}{\sqrt{3}} \quad . \tag{19}$$

A conservative capacitor voltage rating is $1.5V_{out}$.

Diode Ratings – For the diode, a conservative voltage rating is $2V_{in}$ because of the oscillatory ringing transients that invariably occur with parasitic inductances and capacitances. To determine the current rating, examine the graph of diode current shown in Figure 11.
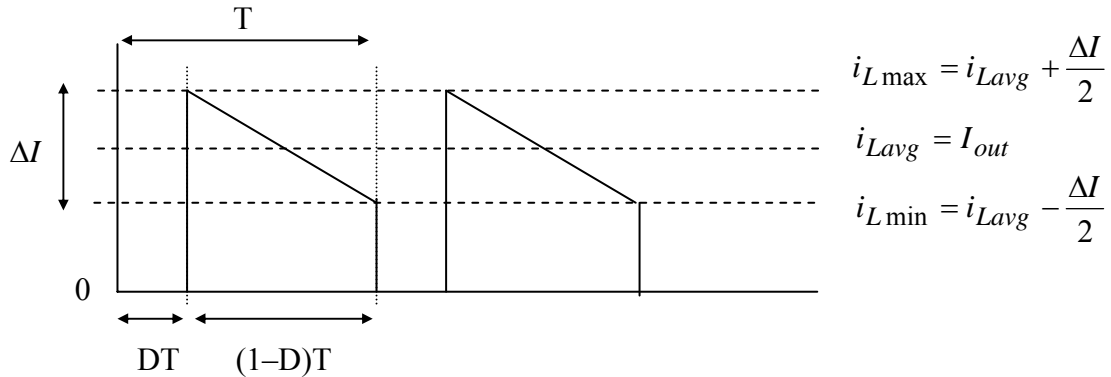
Figure 11. Diode Current Waveform for Continuous Conduction

A conservative assumption for diode current is to assume small D, so that the diode current is essentially the same as the inductor current. Thus, a conservative estimate is that diode rms current equals the inductor rms current given by (17).

MOSFET Ratings – It is clear in Figure 1 that the MOSFET must conduct inductor current when closed, and hold off V_{in} when open. The actual voltage rating of the MOSFET should be at least twice V_{in} to allow for the oscillatory ringing transients that invariably occur. To determine the current rating, examine the graph of the MOSFET current shown in Figure 12.
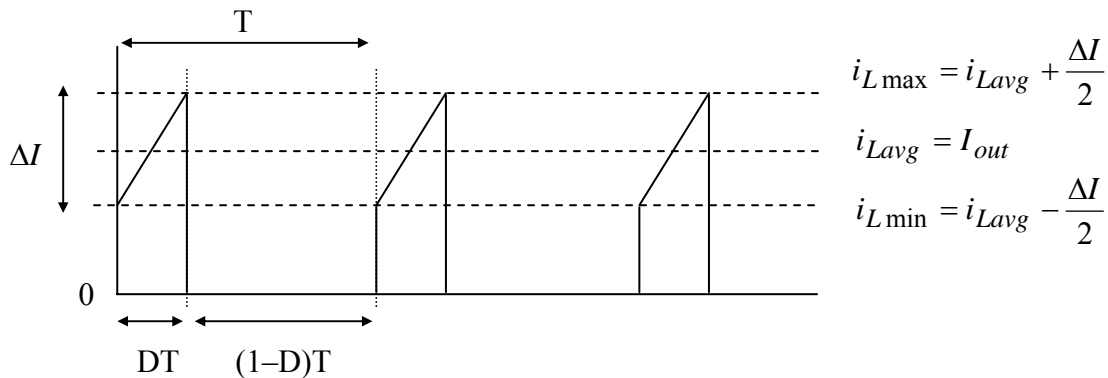
Figure 12. MOSFET Current for Continuous Conduction

A conservative assumption is to assume large D, so that the MOSFET current is essentially the same as the inductor current. Thus, a conservative estimate is that MOSFET rms current equals the inductor rms current given by (17).

The Experiment

Use #16 stranded wire for power wiring (red for +, black for –).

1. Using a 10" long piece of 1" by 6" wood, develop a plan for the layout of the circuit. This board will contain only the buck converter. The MOSFET firing circuit will remain on its own wood piece.

   Keep jumper connections short, ≈ 3 inches or less.
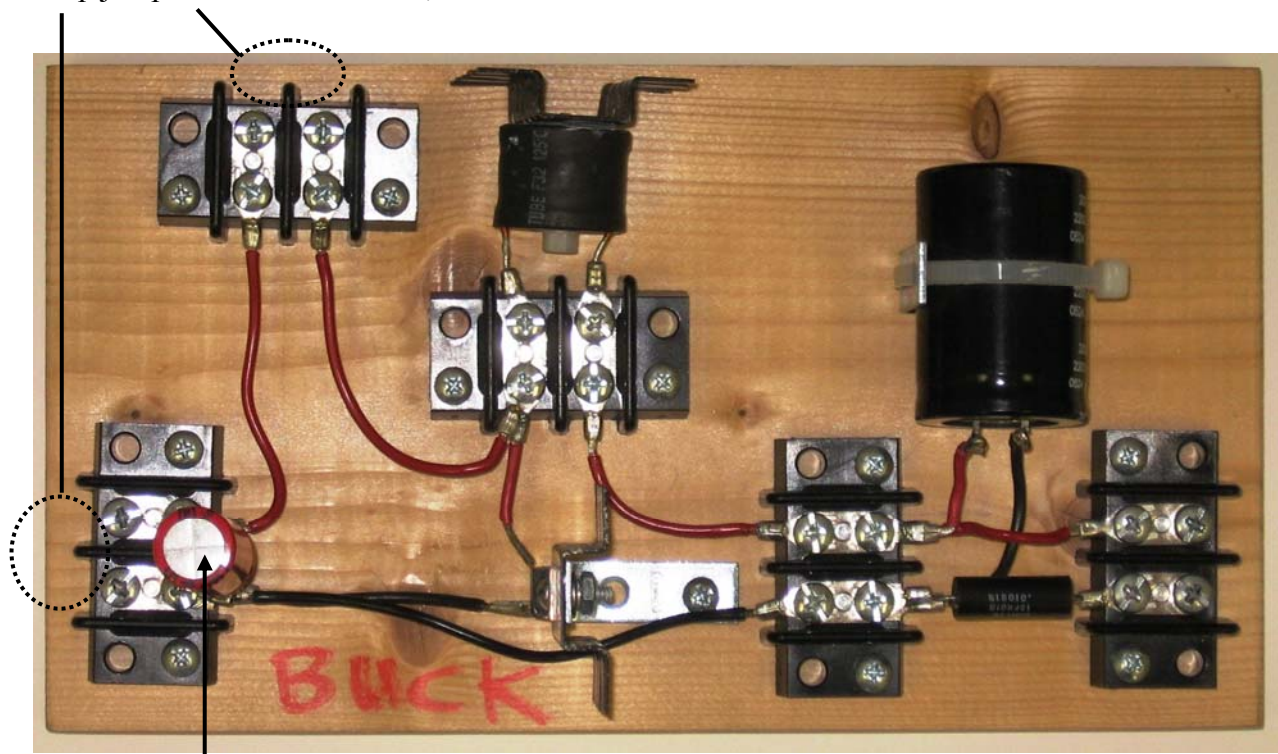
   Mount 10μF ripple current capacitor
   across the input terminals

2. Use the diode feature on your multimeter to identify the anode (P) and cathode (N) leads of the diode.

3. Be sure to use a thin layer of heat sink compound when attaching the inductor and diode to their heat sinks (see next step).

4. Complete the wiring of the circuit in Figure 1, using #16 stranded red and black wire for + and – current carrying connections, respectively. Usually, a wide stripe down the side of a filter capacitor indicates the ground terminal. Secure the filter capacitor to a 1½" steel corner

bracket with a nylon cable tie. Secure the inductor to its heat sink with a nylon screw and nut. Secure the diode and its heat sink to a 1½" steel corner bracket, using a #6-32 x ½" machine screw, flat washer, split washer, and nut. **Be very careful with the diode polarity because, if it is connected backward, it will short circuit the input voltage. Likewise, the filter capacitor is an electrolytic, and it can rupture if connected backward. So be extra careful with capacitor** polarity.

5. Mount a 10µF ripple current capacitor across the V_{in} terminals. (This capacitor will remain in place when you modify your circuit later to become boost and buck/boost converters.)

6. **Do not yet energize your circuit with a DBR.**

7. **Remove and discard the MOSFET snubber capacitor.**

8. Connect a $12V_{dc}$ regulated "wall wart" to the DC jack of a MOSFET firing circuit. Observe V_{GS} on an oscilloscope while varying D and F over their ranges. V_{GS} should have the desired rectangular appearance, and D and F should have the desired ranges.

9. Connect the MOSFET firing circuit to your buck converter, **keeping the wires short (i.e, 3" or less). Do not accidentally connect your buck converter to the MOSFET gate terminal.** Then, connect a 10Ω power resistor as a load.

Important Note: the first time you energize your converter in Step 10, it is a good idea to feed the 120/25V transformer and DBR through a variac. That way, you can gradually increase the voltage and detect short circuits or other problems before they become serious. The ammeter on the variac is an excellent diagnostic tool. Once you are convinced that your circuit is working correctly, then you can remove the variac.

If your circuit has a short in Step 10, then do the following:

1. Make sure that your diode is not connected backwards.
2. Observe V_{GS} on the MOSFET as you vary D and F. Does the waveform look correct?
3. Unplug the wall wart. Does the short circuit go away? If not, your MOSFET may be shorted – so, disconnect the MOSFET from the converter, and perform the voltage-controlled resistance test on the MOSFET.

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10. Connect a $25V_{ac}$ transformer to a DBR. Connect the DBR to your buck converter, **keeping the wires short (i.e., 3" or less)**. Then, energize the $25V_{ac}$ transformer and DBR. If using a variac, adjust the variac so that V_{ac} of the transformer is 27-28V.

11. Using the 10Ω, and with F = 100kHz, adjust D over the range 0.90 to 0.10, in steps of 0.10, while recording V_{in} and V_{out}. Compare the V_{out}/V_{in} ratio to theory, and plot the measured ratios and theoretical ratios versus D on one graph. For D = 0.90, obtain I_{in} and I_{out} by measuring the voltages across the bodies of the 0.01Ω resistors. Multiply to get P_{in} and

P_{out}, and then determine the efficiency of your buck converter. Check to see if your MOSFET, diode, inductor, or output capacitor are "hot."

12. Repeat the above step, using a 5Ω resistor as a load.

13. With 100kHz, D = 0.90, and the 5Ω load, use (5), (6), and (8) to compute inductor rms current. Use (6) and (8), with $I_{avg} = 0$, to compute capacitor rms current.

14. Keeping D = 0.90, lower F to 15-20kHz. Use your oscilloscope to measure the peak-to-peak ripple voltage of V_{in} and V_{out}. Use "averaging with 1 cycle."
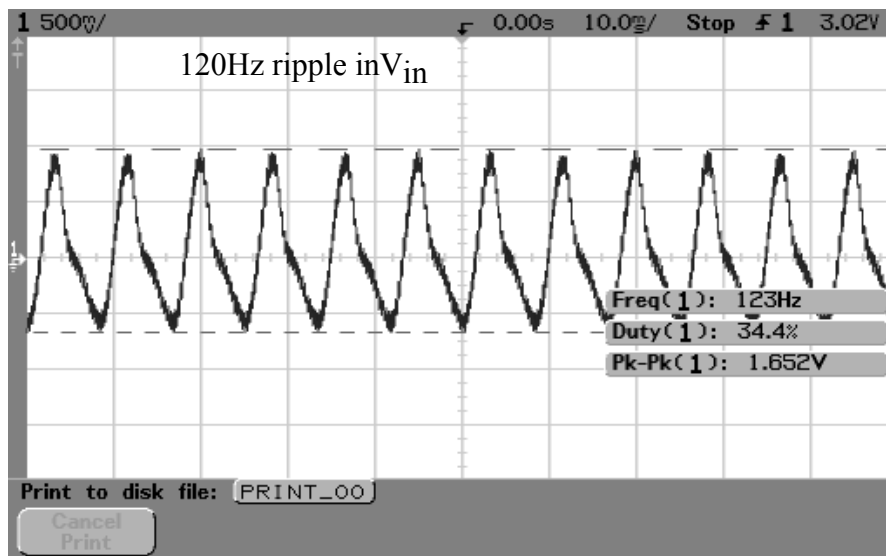
V_{in} Ripple Voltage with 5Ω Load, D = 0.90, F = 15-20kHz
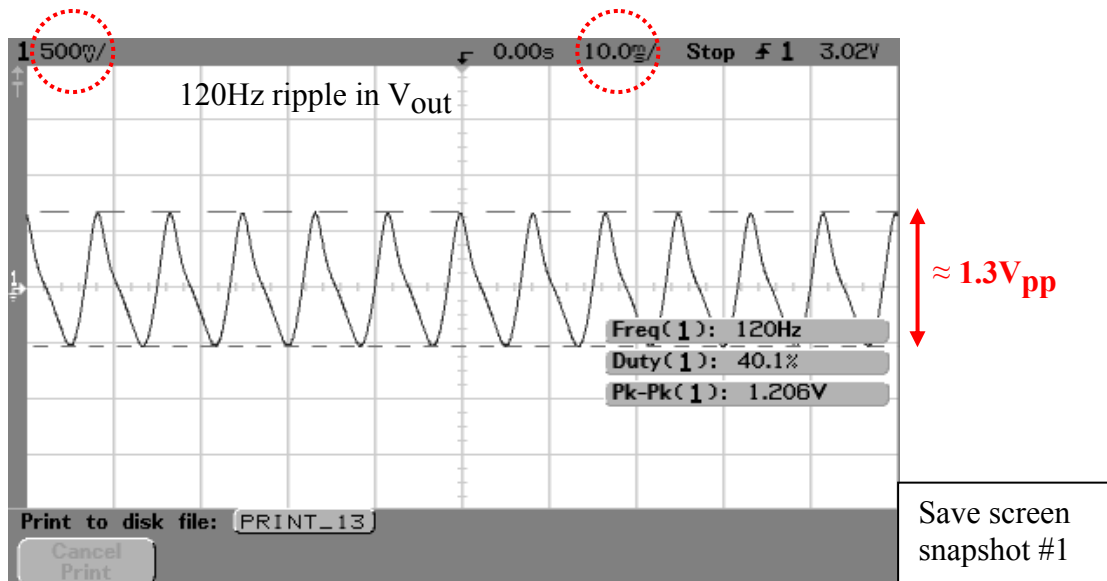
V_{out} Ripple Voltage with 5Ω Load, D = 0.90, F = 15-20kHz

15. Approximating the V_{out} ripple waveform as a triangle wave, estimate its rms value using

$$V_{rms}^2 = \frac{V_{pp}^2}{12}, \quad V_{rms} = \frac{V_{pp}}{\sqrt{12}} = \frac{V_{pp}}{2\sqrt{3}}. \quad \text{(for the example above, the result is } V_{rms} = 0.375V \text{)}$$

Compare the calculation result to that shown by a multimeter "AC" measurement.

16. Zoom-in the time scale to 20μsec/div and observe the 15-20kHz component of V_{out}. Freeze the frame to take out the superimposed 120Hz background ripple. Compare the V_{pp} on the scope to the "worst case" predicted by (14). Repeat the triangle-wave assumption V_{rms} calculation.
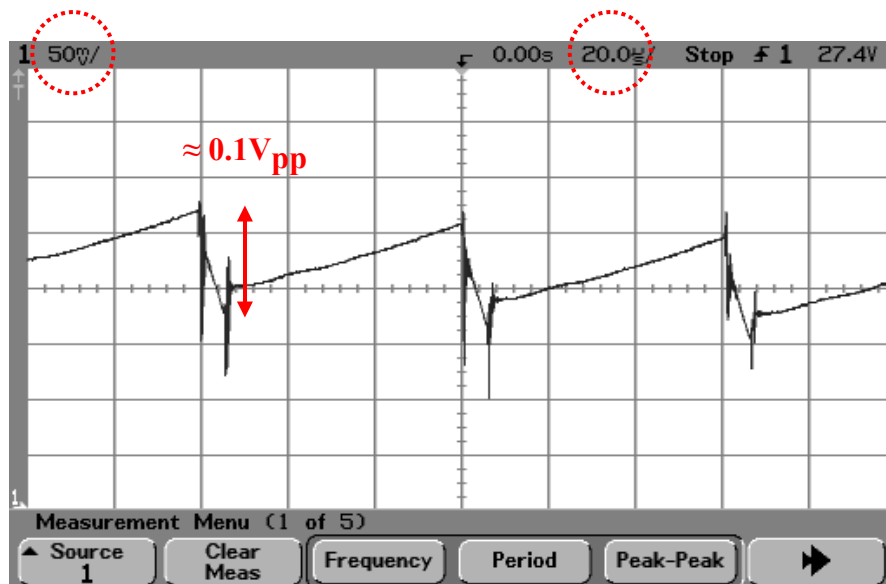
15-20kHz Ripple Component of V_{out}

17. While connected to V_{out}, use the FFT scope feature to determine the magnitude (in volts rms) of the 120Hz and 15-20kHz components. Compare your rms readings to the triangle-wave assumption rms calculations of the previous two steps. How large is the 15-20kHz component compared to the 120Hz component?
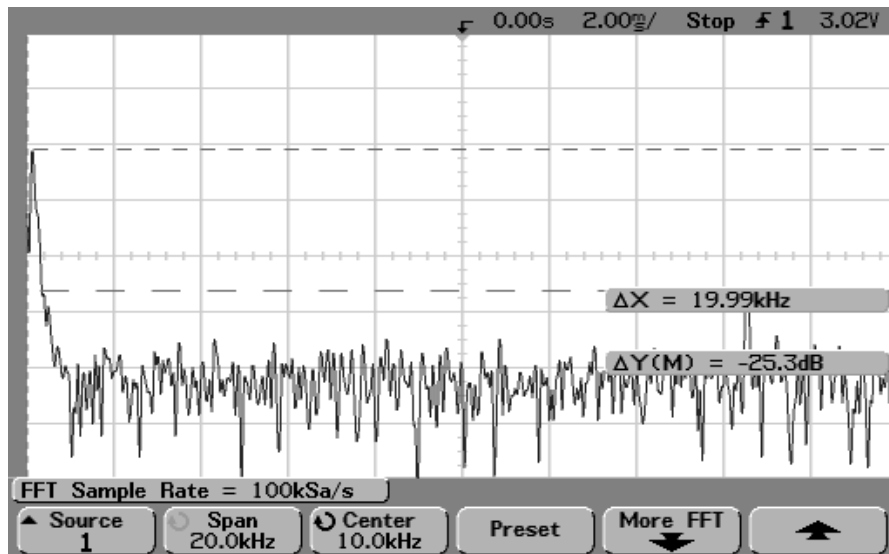
Spectral Content of V_{out} with 5Ω Load, D = 0.90, F = 15-20kHz
(Sample Rate, Span, and Center Frequency Shown)
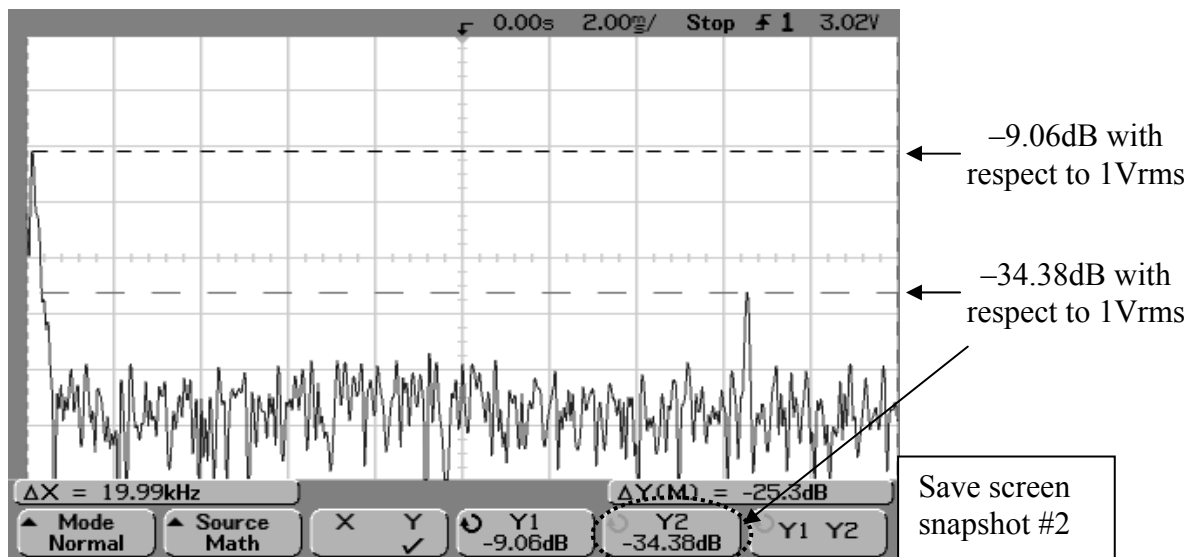
Spectral Content of V_{out} with 5Ω Load, D = 0.90, F = 15-20kHz
(db Values of 120Hz and 16.5kHz Components Shown)

18. Move the oscilloscope probe to view V_{DS}. Measure the peak value of V_{DS} for the following two cases:
   A. without ripple current capacitor, and
   B. with ripple current capacitor.
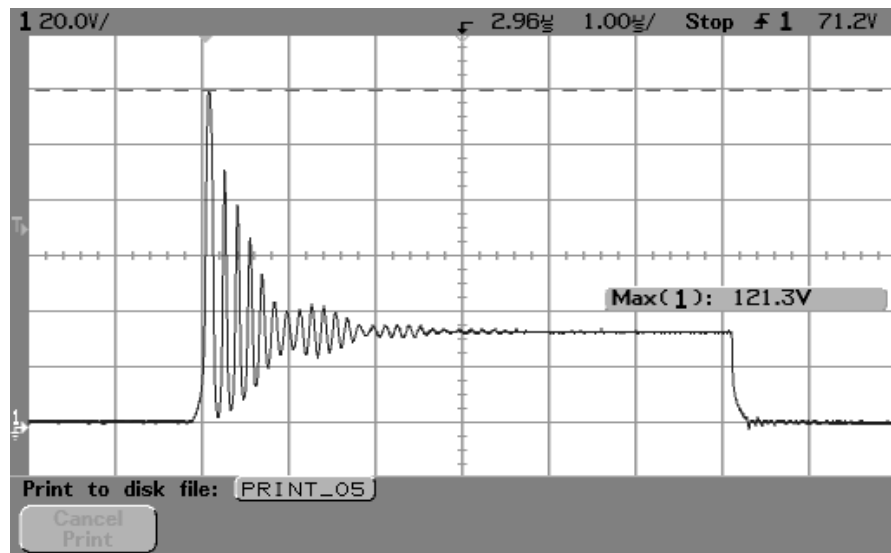
Case A. V_{DS} without Ripple Current Capacitor
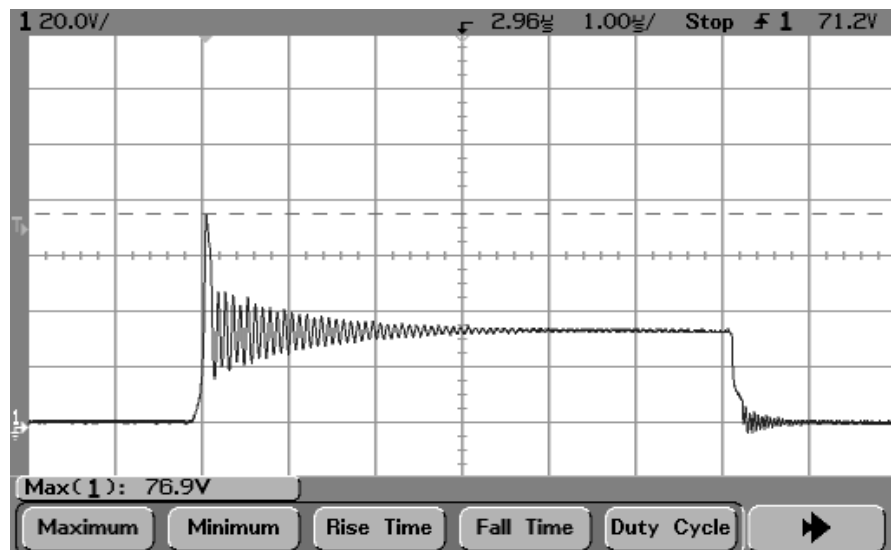
Case B. Effect of Adding Ripple Current Capacitor

19. Move the oscilloscope probe to view the voltage across the inductor (i.e., V_L). Lower D until the onset of discontinuous conduction (denoted by the appearance of a "low frequency" parasitic oscillation in the inductor voltage due to the interaction of L with MOSFET and diode capacitances). Record the values of D, F, V_{in}, I_{in}, V_{out}, and I_{out} at the continuous/discontinuous boundary, and save a screen snapshot that shows the oscillation during discontinuous conduction. Substitute the values into (9) and calculate L. Compare the calculated L to the actual L used in the circuit.
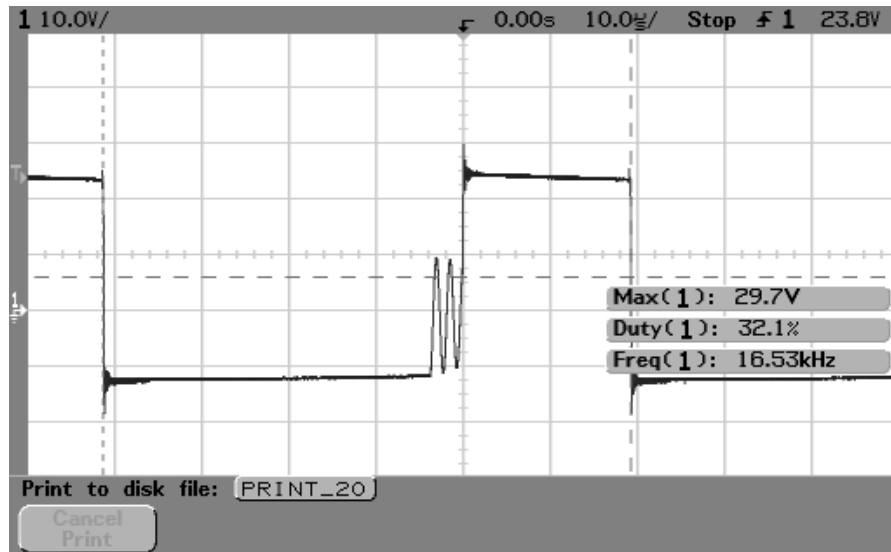
Save screen snapshot #4

V_L during Discontinuous Conduction
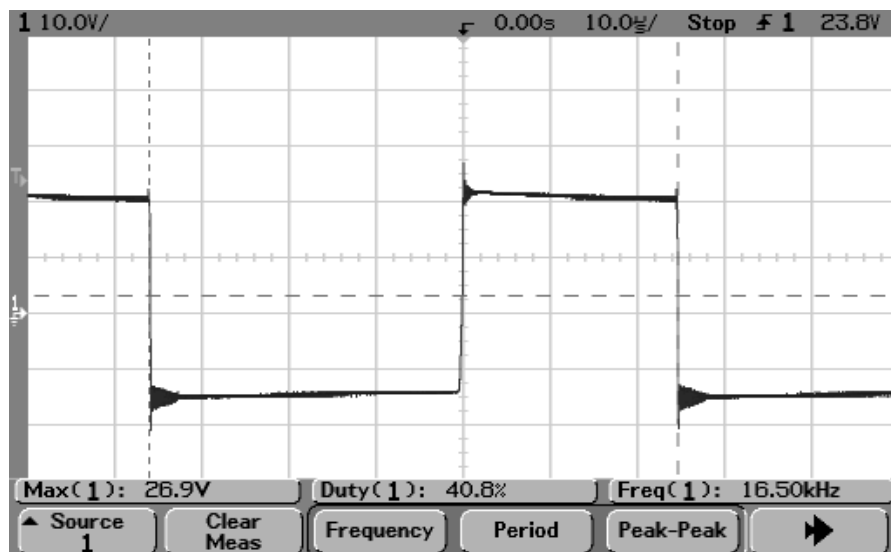
V_L at the Conduction/Discontinuous Boundary

EE462L, Power Electronics, DC-DC Buck Converter
Version Oct. 4, 2010

Parts List

- 200V, 16A ultrafast rectifier (Fairchild Semiconductor FES16DT, Mouser #512-FES16DT).
- Heat sinks for diode and inductor, approx. 1.5" x 1.75" for TO-220 case style, 9.6°C/W (Aavid Thermalloy, Mouser #532-507222B00)
- Output cap is 1500 – 2200µF, 200V – 250V, 5Arms ripple current, electrolytic. (Panasonic #ECE-T2EP152EA, 1500µF, 250V, 5.66Arms ripple at 10kHz-50kHz, Digikey #P10048-ND). **Be careful with polarity**.
- Inductor is 100µH, 9A (J. W. Miller RF Choke, Model 1130-101K-RC, Newark #63K3321 or Mouser #542-1130-101K-RC)
- #4-40 x 1" flat slotted nylon screw and lock nut (Eagle Plastics, Mouser #561-J440-1 and #561-H440, respectively) for mounting the inductor
- One 0.01Ω current sensing resistor (for measuring output current) (in student parts bin).
- 10µF high-frequency bipolar capacitor (50V, 10A peak-to-peak ripple current, Xicon #140-BPHR50V10-RC, Mouser #140-BPHR50V10-RC). **This capacitor is not polarized.**
- Five two-terminal, 30A terminal blocks
- Steel corner brackets (1½" for filter capacitor, and 1½" for diode and its heat sink, holes not enlarged).
- 8" nylon cable tie (Eagle Plastics #481-0115, Mouser # 481-0115) (in student parts bin)
- 1" by 6" wood, 10" long piece

EE462L, Power Electronics, DC-DC Boost Converter
Version Oct. 6, 2010

Overview
Boost converters make it possible to efficiently convert a DC voltage from a lower level to a higher level.

Theory of Operation

Relation Between V_{out} and V_{in} in Continuous Conduction

The idealized boost converter circuit is shown below in Figure 1. Under normal operation, the circuit is in "continuous conduction" (i.e., i_L is never zero)

Remember – never connect a variac directly to a DBR!

Leave the 10µF cap across the input terminals
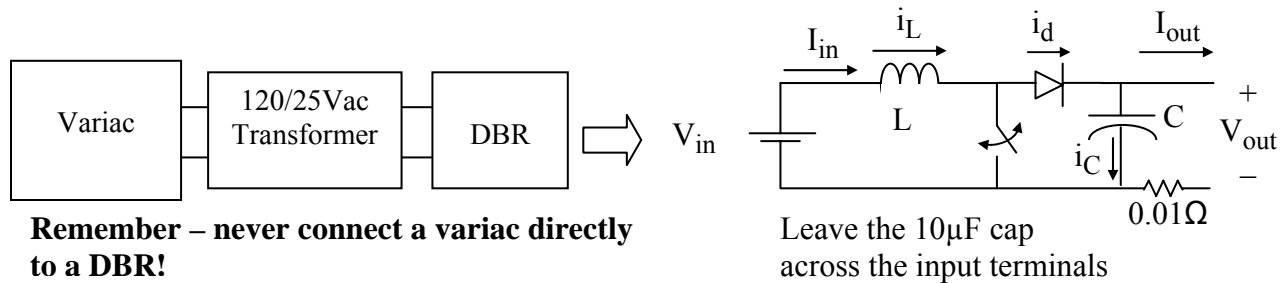
Figure 1. DC-DC Boost Converter

The circuit is assumed to be lossless so that $P_{in} = P_{out}$, or

$$V_{in} \bullet i_{Lavg} = V_{out} \bullet I_{out} \text{ , where } i_{Lavg} = I_{in} \text{ .}$$ (1)

Assuming continuous conduction, the circuit has two topologies – switch closed, and switch open. Both are shown in Figures 2a and 2b.
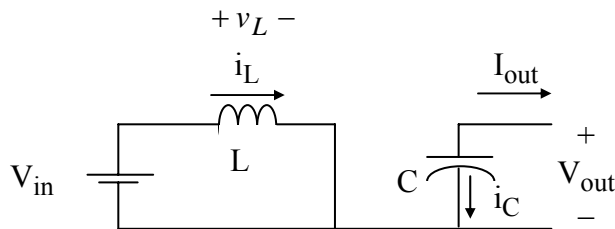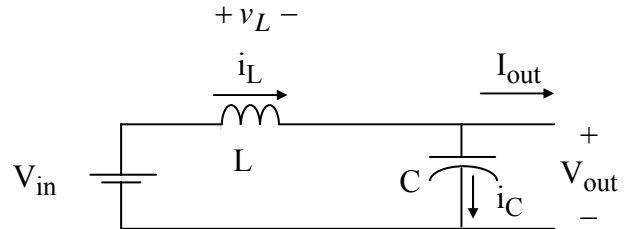
Figure 2a. Switch Closed for DT Seconds

Figure 2b. Switch Open for (1-D)T Seconds (Continuous Conduction)

When the switch is closed, the diode is reverse biased and open, and i_L increases at the rate of

$$\frac{di_L}{dt} = \frac{v_L}{L} = \frac{V_{in}}{L}, \ 0 \le t \le DT ,$$ (2)

and the inductor is "charging." When the switch is open, the diode is forward biased, and i_L decreases at the rate of

$$\frac{di_L}{dt} = \frac{v_L}{L} = \frac{V_{in} - V_{out}}{L}, \; DT < t < T \; , \tag{3}$$

and the inductor is "discharging." The inductor voltage is shown in Figure 3.
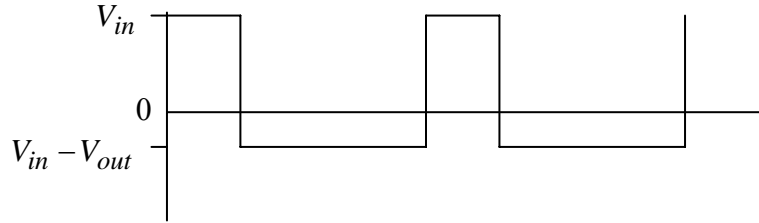
Figure 3. Inductor Voltage in Continuous Conduction

Because of the steady-state inductor principle, the average voltage v_L across L is zero. Since v_L has two states, both having constant voltage, the average value is

$$\frac{(V_{in})DT + (V_{in} - V_{out})(1-D)T}{T} = 0,$$

so that

$$V_{in}D + V_{in} - V_{out} - V_{in}D + V_{out}D = 0 \; .$$

Simplifying the above yields the final input-output voltage expression

$$V_{out} = \frac{V_{in}}{1-D} \; . \tag{4}$$

Inductor Current in Continuous Conduction

The graph of i_L is shown in Figure 4.

$$i_{L\max} = i_{Lavg} + \frac{\Delta I}{2}$$

$$i_{Lavg}$$

$$i_{L\min} = i_{Lavg} - \frac{\Delta I}{2}$$
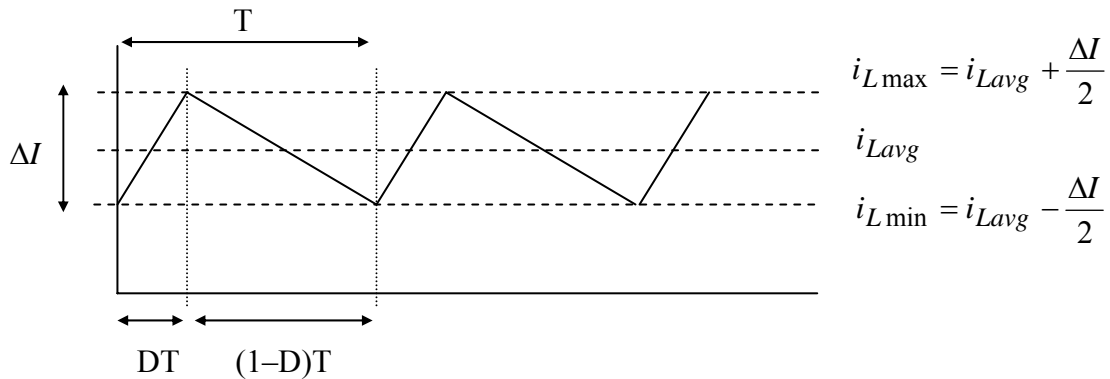
Figure 4. Inductor Current Waveform for Continuous Conduction

From (2),

$$\frac{di_L}{dt} = \frac{V_{in}}{L} = \frac{\Delta I}{DT},$$

so that

$$\Delta I = \frac{V_{in}}{L} \bullet DT = \frac{V_{in}D}{Lf}, \tag{5}$$

where f is the switching frequency.

The boundary of continuous conduction is when $i_{L\min} = 0$, as shown in Figure 5.
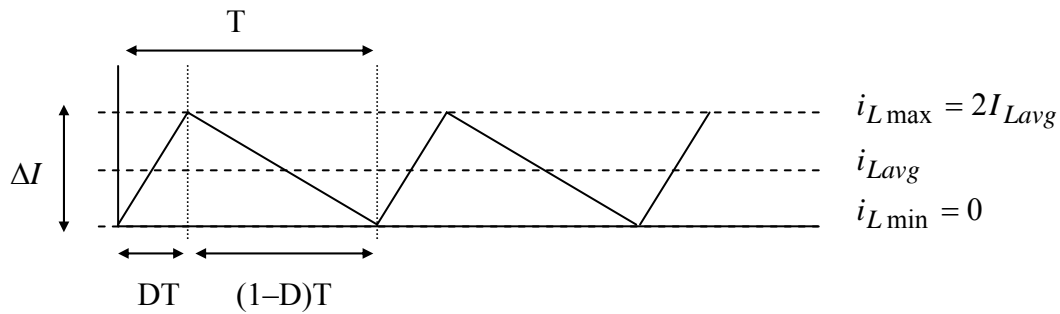
Figure 5. Inductor Current at the Boundary of Continuous Conduction

Using Figure 5 and the "inductor discharging" slope from (3),

$$\Delta I = \frac{(V_{out} - V_{in})(1 - D)}{L_{boundary}f} = \frac{V_{in} - V_{in}(1 - D)}{L_{boundary}f} = \frac{V_{in}D}{L_{boundary}f} = 2I_{Lavg}, \tag{6}$$

so that

$$L_{boundary} = \frac{V_{in}D}{2I_{Lavg}f}. \tag{7}$$

From (1),

$$I_{Lavg} = I_{in}. \tag{8}$$

Substituting into (8) into (7) yields

$$L_{boundary} = \frac{V_{in}D}{2I_{in}f} \ . \tag{9}$$

Because the maximum value of D is 1, then

$$L > \frac{V_{in}}{2I_{in}f} \ . \tag{10}$$

will guarantee continuous conduction for all D. Note in (9) and (10) that continuous conduction can be achieved more easily when I_{out} and f are large.

Discontinuous Conduction

At low load, the converter may slip into the discontinuous conduction mode. Referring back to Figure 2b, this occurs when the inductor current coasts to zero. At that moment, the capacitor attempts to reverse i_L and "backfeed" the inductor, but the diode prevents current reversal. Thus, the diode opens, and the circuit assumes the topology shown in Figure 6 until the switch closes again. During this third state, all load power is provided by the capacitor.
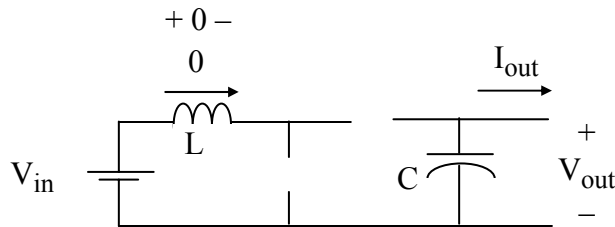
Figure 6. Third State for Discontinuous Conduction

Once discontinuous, the voltage across the inductor is zero. The corresponding voltage waveform is shown in Figure 7.
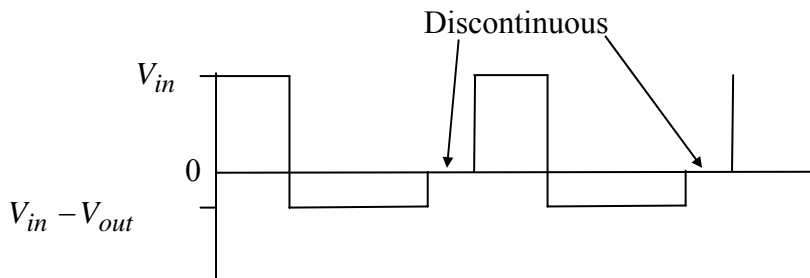
Figure 7. Inductor Voltage in Discontinuous Conduction

Current Waveforms in Continuous Conduction

Continuous current waveforms are shown below.

Inductor

$$i_{L\max} = i_{Lavg} + \frac{\Delta I}{2}$$

$$i_{Lavg} = I_{in}$$

$$i_{L\min} = i_{Lavg} - \frac{\Delta I}{2}$$

ΔI

T

DT   (1–D)T

MOSFET

$$i_{L\max} = i_{Lavg} + \frac{\Delta I}{2}$$

$$i_{Lavg} = I_{in}$$

$$i_{L\min} = i_{Lavg} - \frac{\Delta I}{2}$$

ΔI

0

Diode

$$i_{L\max} = i_{Lavg} + \frac{\Delta I}{2}$$

$$i_{Lavg} = I_{in}$$

$$i_{L\min} = i_{Lavg} - \frac{\Delta I}{2}$$

ΔI

0

Capacitor $(i_C = i_L - I_{out})$

$$i_{Lavg} + \frac{\Delta I}{2} - I_{out}$$

$$i_{Lavg} - I_{out} = I_{in} - I_{out}$$

$$i_{Lavg} - \frac{\Delta I}{2} - I_{out}$$

$$-I_{out}$$

ΔI

0
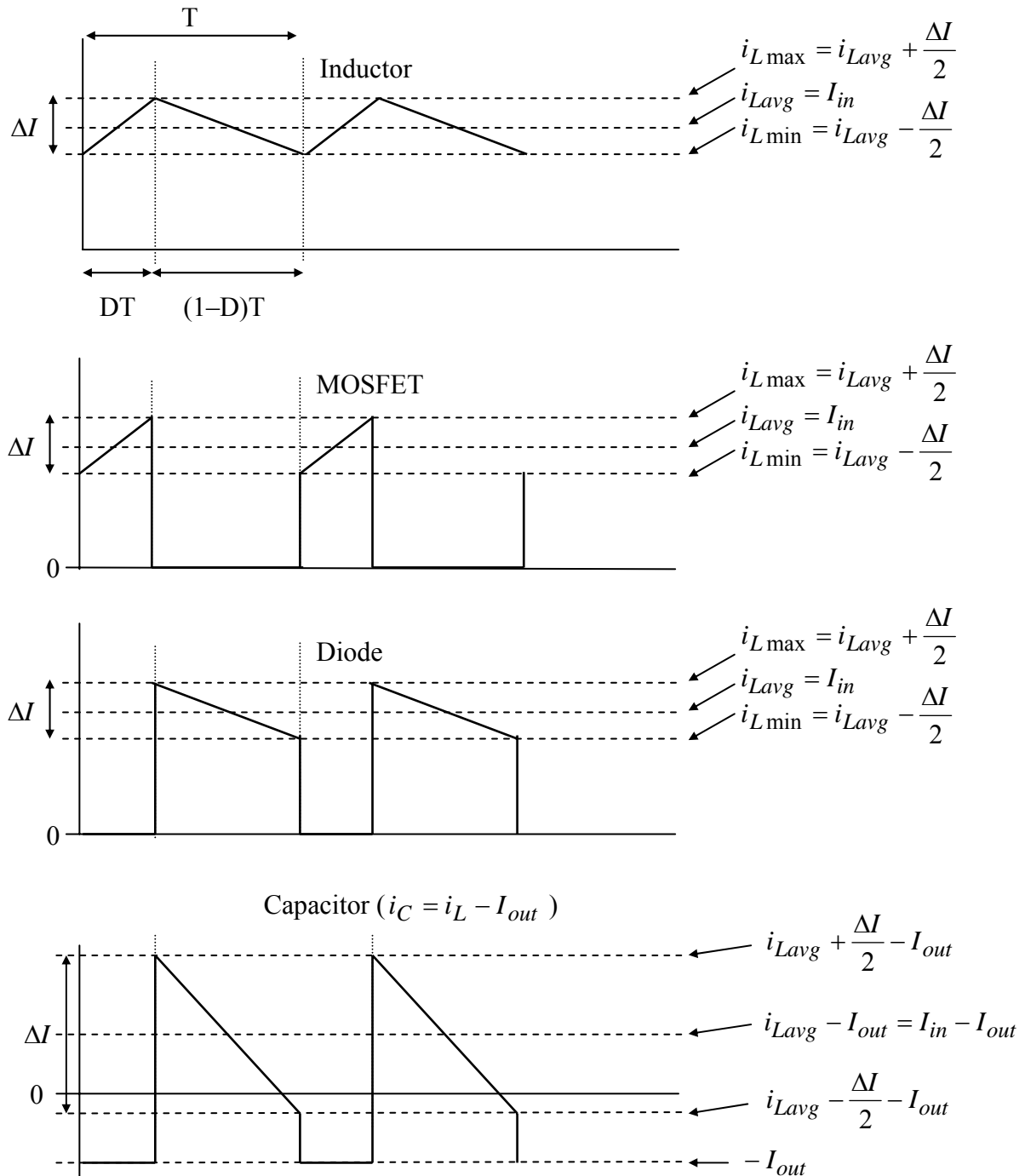
(Note – compared to the other waveforms shown above, ΔI is exaggerated in the figure to illustrate how the capacitor current can be negative in both DT and (1–D)T regions)

Figure 8. Current Waveforms for Continuous Conduction

Current Ratings in Continuous Conduction

Conservative current ratings for the inductor in continuous conduction correspond to the situation where

$$\Delta I_{\max} = 2I_{in}, \tag{11}$$

which, as explained in the Buck Converter experiment, yields

$$I_{Lrms,\max}^2 = I_{in}^2 + \frac{1}{12}(2I_{in})^2 = I_{in}^2\left(1 + \frac{1}{3}\right), \tag{12}$$

so that

$$I_{Lrms,\max} = \frac{2}{\sqrt{3}} I_{in}. \tag{13}$$

Conservative current ratings for the MOSFET and diode are when D is large, so that (13) applies for them also.

To determine the rms current through C, consider the capacitor current in Figure 8, and the worst-case scenario in Figure 9.
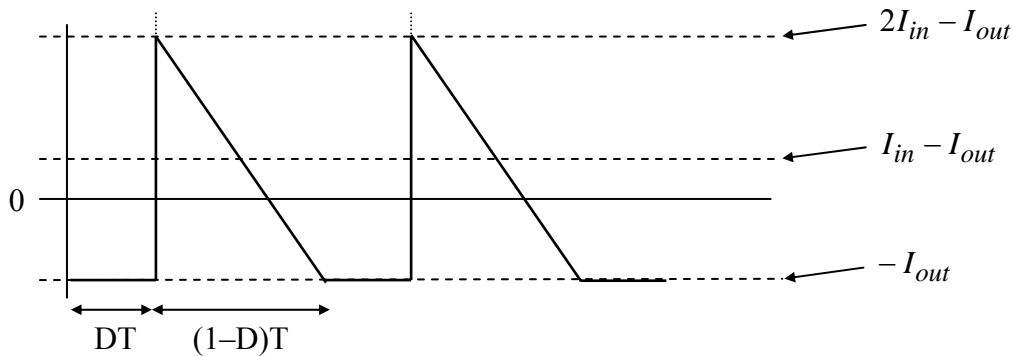
Figure 9. Maximum Ripple Current Case for Capacitor Current

When the switch is closed, the capacitor current is $-I_{out}$. When the switch is open, the capacitor current is $i_L - I_{out}$. If the "switch closed" interval lasted for the entire T, the squared rms value would be I_{out}^2. If the "switch open" interval lasted for the entire T, the rms value would be, for the maximum ripple case, $(I_{in} - I_{out})^2 + \frac{1}{12}(2I_{in})^2$. The time-weighted average of the two gives the squared rms current

$$I_{Crms}^2 = DI_{out}^2 + (1-D) \bullet \left((I_{in} - I_{out})^2 + \frac{1}{12}(2I_{in})^2 \right). \tag{14}$$

Now, substituting in $I_{out} = I_{in}(1-D)$ yields

$$I_{Crms}^2 = DI_{in}^2(1-D)^2 + (1-D) \bullet \left((I_{in} - I_{in}(1-D))^2 + \frac{1}{12}(2I_{in})^2 \right).$$

Simplifying yields

$$I_{Crms}^2 = DI_{in}^2(1-D)^2 + (1-D) \bullet \left(I_{in}^2 D^2 + \frac{1}{3}I_{in}^2 \right),$$

$$I_{Crms}^2 = I_{in}^2 \left(D(1-D)^2 + (1-D)D^2 + \frac{(1-D)}{3} \right),$$

$$I_{Crms}^2 = I_{in}^2 \left(\frac{-3D^2 + 2D + 1}{3} \right),$$

Setting the partial derivative with respect to D shows that the maximum occurs at $D = \frac{1}{3}$, which yields

$$I_{Crms,max} = \frac{2}{3}I_{in}.$$

Since D = , then substituting for I_{in} yields

$$I_{Crms,max} = \frac{2}{3} \bullet \frac{I_{out}}{\left(1 - \frac{1}{3}\right)} = I_{out}. \tag{15}$$

Voltage Ratings for Continuous Conduction

Referring to Figure 2b, when the MOSFET is open, it is subjected to V_{out}. Because of the usual double-voltage switching transients, the MOSFET should therefore be rated $2V_{out}$.

Referring to Figure 2a, when the MOSFET is closed, the diode is subjected to V_{out}. The diode should be conservatively rated $2V_{out}$.

Capacitor Voltage Ripple

Re-examining the capacitor current in Figure 9, and re-illustrated in Figure 10, it can be seen that the amount of charge taken from C when the switch is closed is represented by the dotted area.
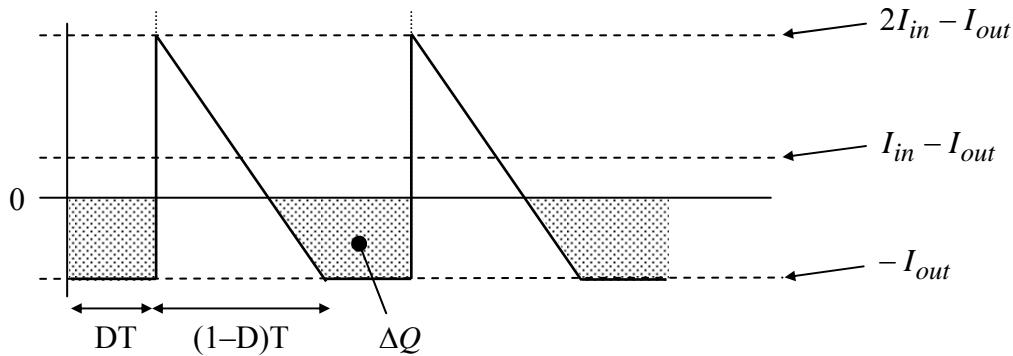
Figure 10. Capacitor Charge Given Up While Switch is Closed

As $D \rightarrow 1$, the width of the dotted area increases to fill almost the entire cycle, and the maximum peak-to-peak ripple becomes

$$\Delta V_{\max} = \frac{I_{out} \bullet T}{C} = \frac{I_{out}}{Cf}. \tag{16}$$

The Experiment (Important - to avoid high output voltages, always keep a load attached to the boost converter output when input power is applied. Use a conventional 120V, 150W light bulb as your load. Do not exceed 120V on the output.

1.   Convert a buck converter to a boost converter, using the circuit shown in Figure 1 of this document.

2.   Double-check that the polarity of your converter's output capacitor is correct.

3.   Locate one of the 150W light bulb test load assemblies. Check the light bulb with an ohmmeter to make sure it is not burned out.

4.   Connect the light bulb test load to your circuit.

5.   Connect an oscilloscope Channel #1 to view V_{GS}, and Channel #2 to view V_{DS}. The ground clip of the Channel #2 probe should not be attached to the circuit, but instead it should be clipped back onto its own lead in-cable so that it does not dangle.

6. **Do not connect a DBR yet**. Connect a MOSFET firing circuit to your converter, **using short wires**, and then power-up your MOSFET firing circuit. Set the oscilloscope to trigger on Channel #1. Observe your oscilloscope to confirm that the controls are working properly.

7. **Set D to the minimum setting**, and F ≈ 100kHz.

Important Note: the first time you energize your boost converter, feed the 120/25V transformer through a variac to the DBR, so that you can SLOWLY increase the voltage from zero and read the variac ammeter to detect short circuits before they become serious. A common problem is to have the MOSFET in backward, so that its internal antiparallel diode creates a short circuit. The ammeter on the variac is an excellent diagnostic tool. Once you are convinced that your circuit is working correctly, the variac is then optional. **Remember – your boost converter requires DC input power from a DBR.**

Does your circuit have a short? If so, do the following:

1. Make sure that your MOSFET is not connected backwards.
2. Observe V_{GS} on the MOSFET as you vary D. Does the waveform look correct?
3. Unplug the wall wart. Does the short circuit go away? If not, your MOSFET may be shorted – so, disconnect the MOSFET from the converter, and perform the voltage-controlled resistance test on the MOSFET, or use the MOSFET tester.

---

8. Connect a variac to a $25V_{ac}$ transformer, and $25V_{ac}$ transformer to a DBR. Connect the DBR to your boost converter, **keeping the wires short**. Then, energize the $25V_{ac}$ transformer and DBR. Slowly raise the variac, checking for a short circuit, so that V_{ac} of the transformer is approximately 27-28V.

9. With F ≈ 100kHz, **slowly** raise D so that Vout increases in steps of about 10V up to 120V, measuring D, V_{in}, I_{in}, $V_{out,}$ and I_{out} as you go. Save a screen snapshot of V_{DS} for V_{out} = 120V that shows the peak value of V_{DS}. Let the circuit run at the $120V_{out}$ condition for 1 or 2 more minutes, and then **turn off your circuit**.
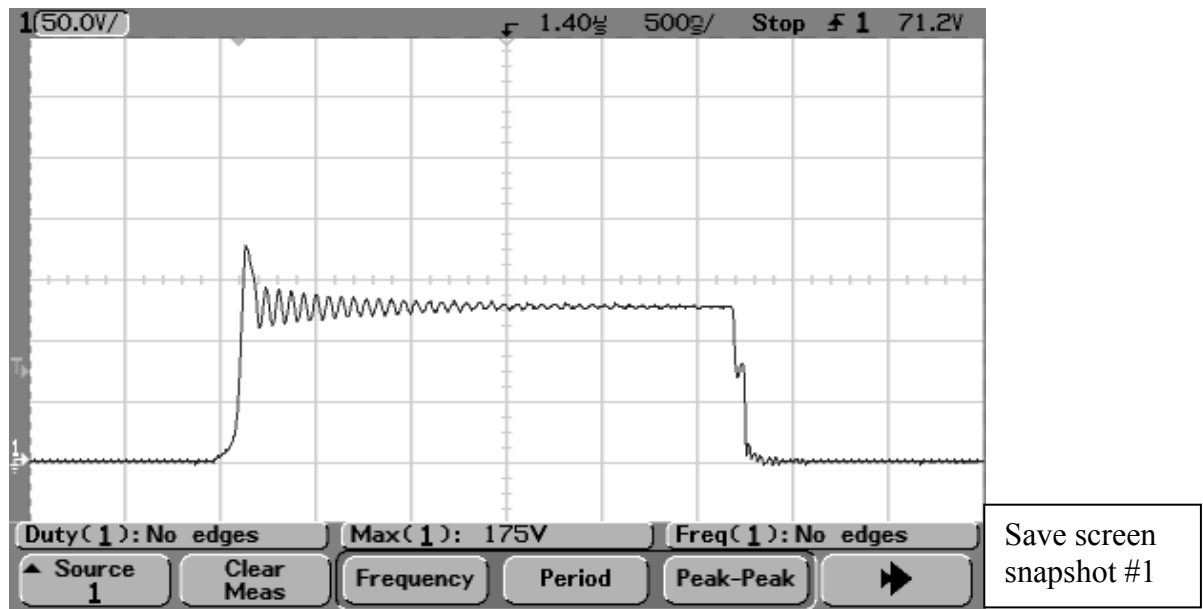
V_{DS} for 90kHz, 120V

10.   **With your circuit turned off**, quickly and carefully use your hand to check MOSFET heat sink temperature and any other hot components. You can also use an infrared thermometer for this step.

11.   Compare your measured V_{out}/V_{in} to theory. Multiply voltages and currents to compute input and output powers, and then compute the efficiency of your circuit for each V_{out} measured. Plot your results in your written report.

12.   When the sun is good, power your converter with a solar panel pair. With a 150W light bulb connected as a load, sweep D to find the maximum power point. Compute the maximum power point value of $R_{load} = V_{out}/I_{out}$ and the corresponding equivalent max power resistance seen by the solar panels. Does the ratio of R_{load} resistance to equivalent resistance seem by the solar panels check with D?
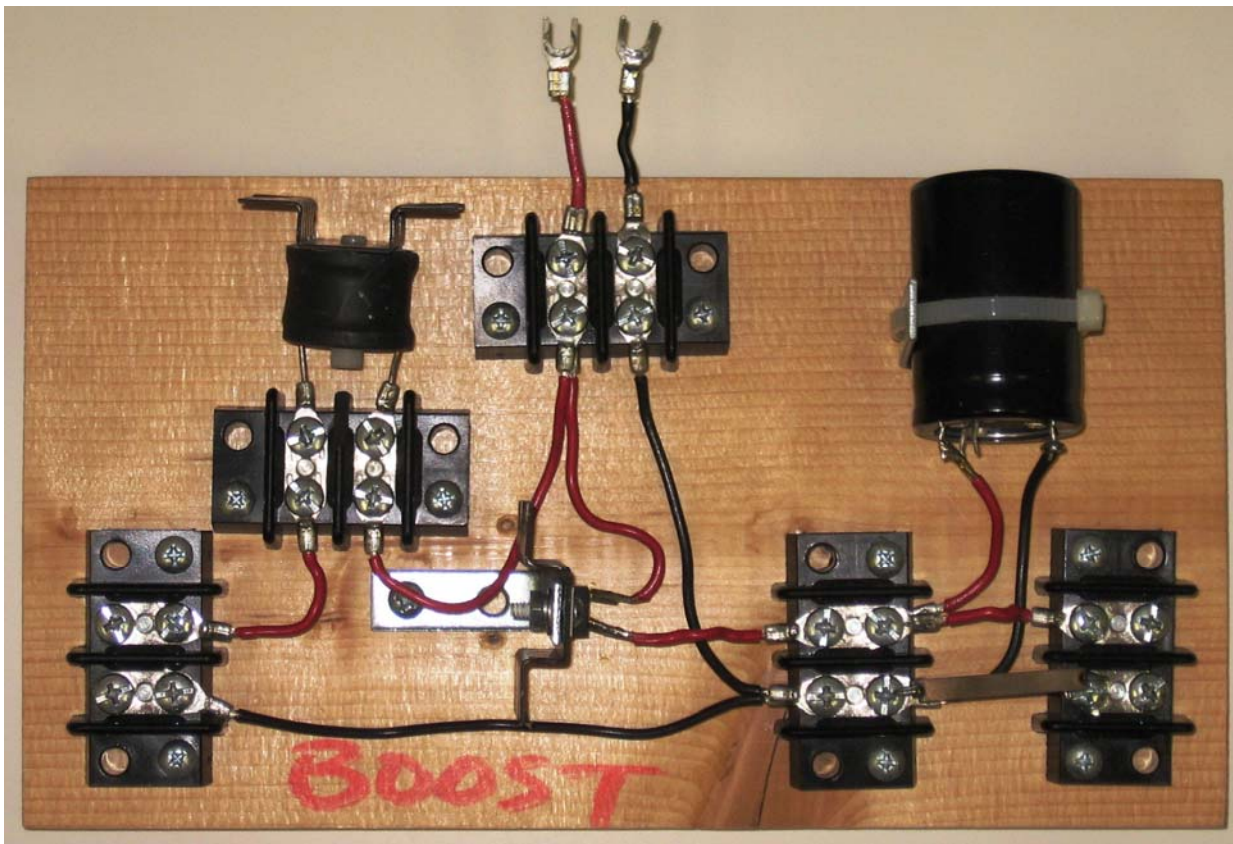
Overview
Buck/Boost converters make it possible to efficiently convert a DC voltage to either a lower or higher voltage. Buck/Boost converters are especially useful for PV maximum power tracking purposes, where the objective is to draw maximum possible power from solar panels at all times, regardless of the load.

Theory of Operation

Relation Between V_{out} and V_{in} in Continuous Conduction

The idealized buck/boost converter circuit is shown below in Figure 1. Under normal operation, the circuit is in "continuous conduction" (i.e., i_{L1} and i_{L2} are always greater than zero).

Remember – never connect a variac directly to a DBR!

Leave the 10µF cap across the input terminals
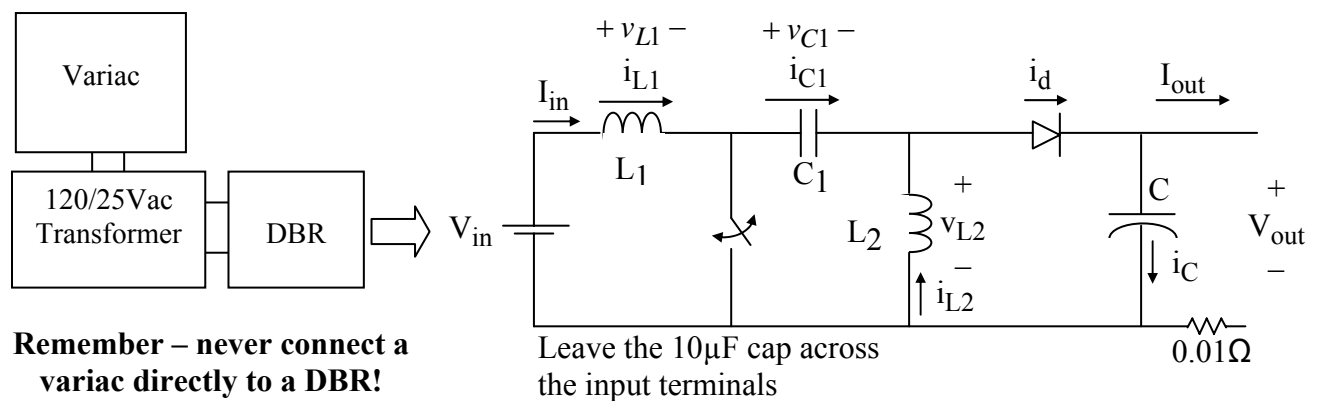
Figure 1. DC-DC Buck/Boost Converter

The first important relationship comes from the fact that capacitor C_1 should be large enough so that voltage v_{C1} has low ripple. Applying average KVL around the loop formed by V_{in}, L_1, C_1, and L_2, and recognizing that the average voltages across L_1 and L_2 are each zero, yields

$$v_{C1} = V_{in} \ . \tag{1}$$

The second important relationship comes by applying KCL in the average sense at the node atop L_2. Since the average currents in C_1 and C are both zero, then

$$i_{L2avg} = i_{davg} = I_{out} \ . \tag{2}$$

With continuous conduction, the circuit has two states – switch closed, and switch open. These states are shown in Figures 2a and 2b.
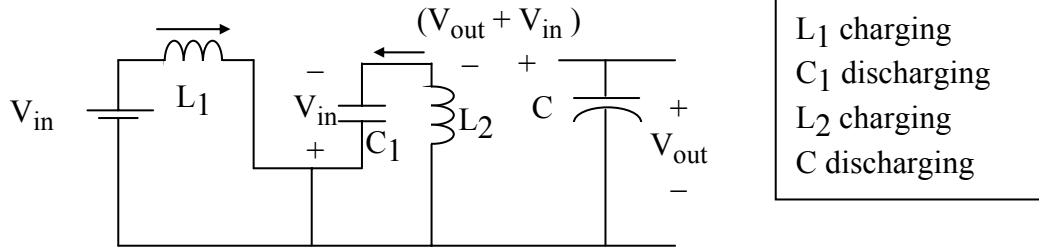
Figure 2a. Switch Closed for DT Seconds
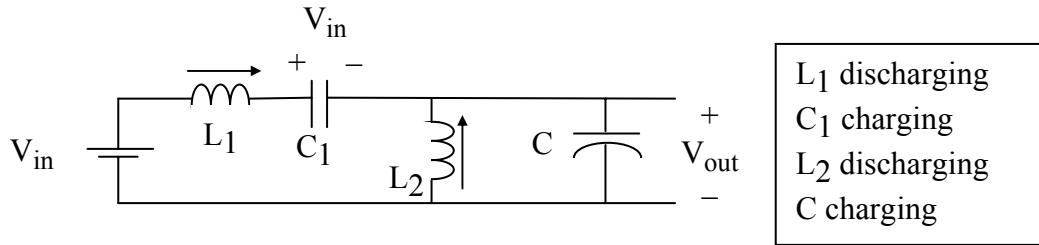
Figure 2b. Switch Open for (1-D)T Seconds

When the switch is closed (Figure 2a), the diode is reverse biased and open, current i_{L1} increases at the rate of

$$\frac{di_{L1}}{dt} = \frac{V_{in}}{L_1}, \ 0 \le t \le DT, \tag{3}$$

so that L_1 is "charging." When the switch is open (Figure 2b), the diode is forward biased, and i_L decreases at the rate of

$$\frac{di_{L1}}{dt} = \frac{-V_{out}}{L_1}, \ DT < t < T, \tag{4}$$

so that L_1 is "discharging." The voltage across L_1 is shown in Figure 3.
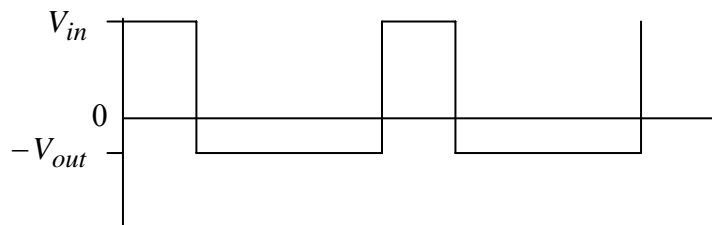
Figure 3. Inductor L_1 Voltage in Continuous Conduction

Because of the steady-state inductor principle, the average voltage across L_1 is zero. Since v_{L1} has two states, both having constant voltage, the average value of v_{L1} is

$$\frac{(V_{in})DT + (-V_{out})(1-D)T}{T} = 0 \, ,$$

so that

$$V_{in}D - V_{out} + V_{out}D = 0 \, . \tag{5}$$

Simplifying the above yields the final input-output voltage expression

$$V_{out} = \frac{DV_{in}}{1-D} \, . \tag{6}$$

Thus, the converter is in "buck" mode for $D < 0.5$, and in "boost" mode for $D > 0.5$.

The assumption of a lossless circuit requires input power to equal output power, so

$$I_{out} = \frac{(1-D)I_{in}}{D} \, . \tag{7}$$

Inductor Currents in Continuous Conduction

The graph of i_{L1} is shown in Figure 4. For PV applications, it is obviously desirable to have low ripple in i_{L1} to keep the solar panel operating at the peak of its maximum power curve.

$$i_{L1\,max} = i_{L1avg} + \frac{\Delta I_1}{2}$$

$$i_{L1avg} = I_{in}$$

$$i_{L1\,min} = i_{L1avg} - \frac{\Delta I_1}{2}$$
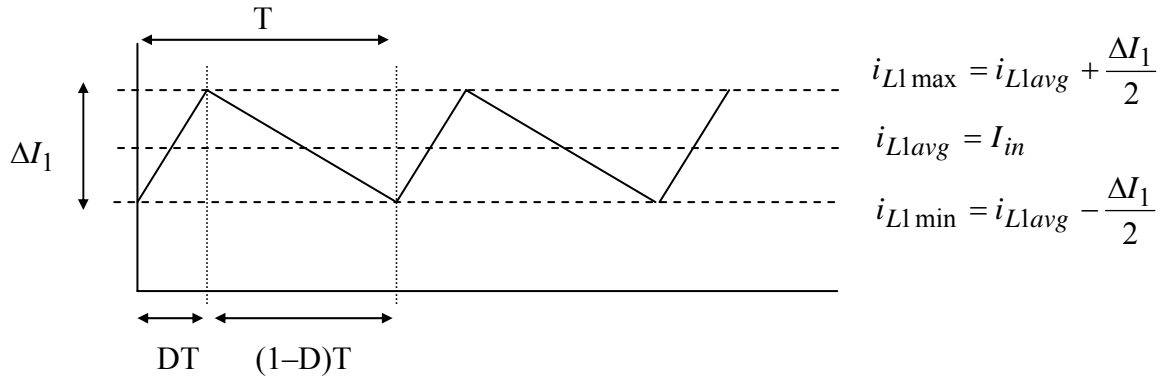
Figure 4. Inductor L_1 Current Waveform for Continuous Conduction

From Figure 4 and Equation (3), when the switch is open (i.e., L_1 is "discharging"),

$$\frac{di_{L1}}{dt} = \frac{-V_{out}}{L_1} \, ,$$

so that

$$\Delta I_1 = \frac{V_{out}}{L_1} \bullet (1-D)T = \frac{V_{out}(1-D)}{L_1 f} \quad , \tag{8}$$

where f is the switching frequency.

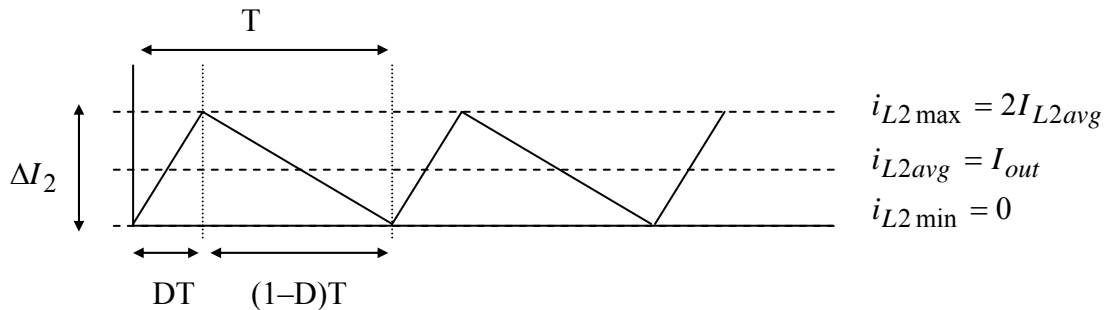The boundary of continuous conduction for L_1 is when $i_{L1\,min} = 0$, as shown in Figure 5.
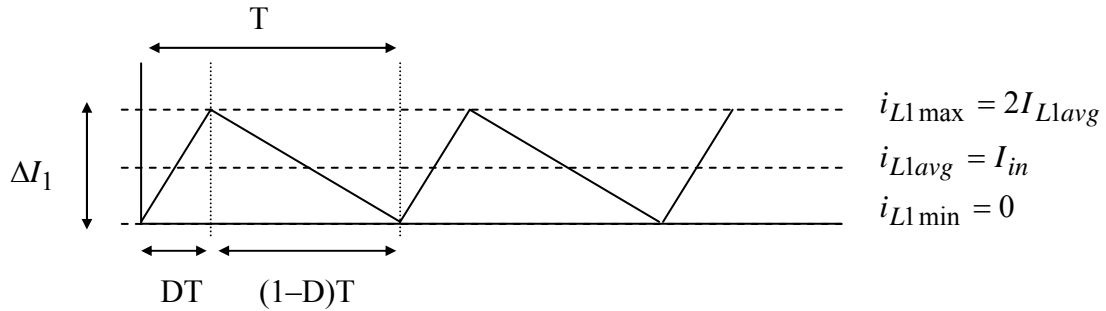
Figure 5. Inductor L_1 Current at the Boundary of Continuous Conduction

Thus, at the boundary,

$$2I_{in} = \frac{V_{out}(1-D)}{L_{1boundary} f} \quad , \tag{9}$$

so that

$$L_{1boundary} = \frac{V_{out}(1-D)}{2I_{in} f} = \frac{DV_{in}}{1-D} \bullet \frac{(1-D)}{2I_{in} f} = \frac{DV_{in}}{2I_{in} f} \quad . \tag{10}$$

As D approaches unity,

$$L_1 > \frac{V_{in}}{2I_{in} f} \tag{11}$$

will guarantee continuous conduction. Note in (10) and (11) that continuous conduction can be achieved more easily when I_{in} and f are large.

The graph of i_{L2} is shown in Figure 6.
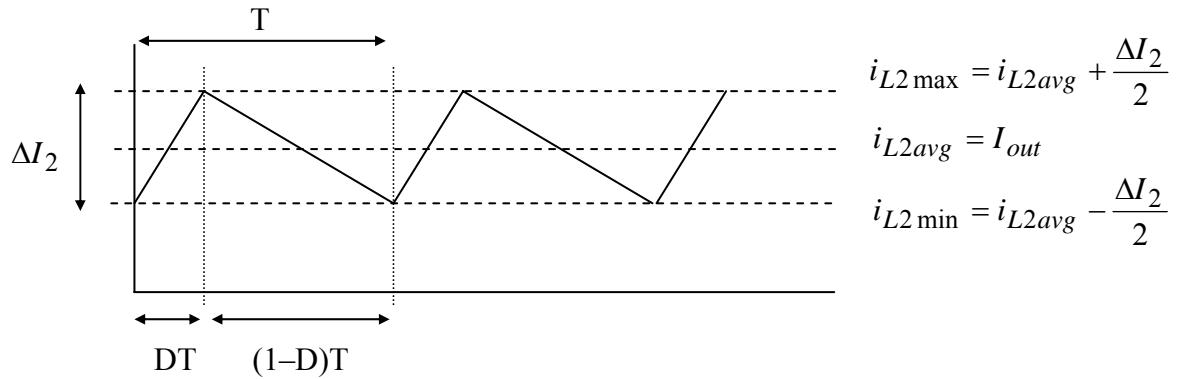
Figure 6. Inductor L_2 Current Waveform for Continuous Conduction

From Figures 2b and 6, when the switch is open (i.e., L_2 is "discharging"),

$$\frac{di_{L2}}{dt} = \frac{-V_{out}}{L_2} = \frac{\Delta I_2}{(1-D)T},$$

so that

$$\Delta I_2 = \frac{-V_{out}(1-D)T}{L_2} = \frac{-V_{out}(1-D)}{L_2 f}, \qquad (12)$$

where f is the switching frequency.

The boundary of continuous conduction for L_2 is when $i_{L2\,min} = 0$, as shown in Figure 7.

Figure 7. Inductor L_2 Current at the Boundary of Continuous Conduction

Thus, at the boundary,

$$2I_{out} = \frac{V_{out}(1-D)}{L_{2boundary} f}, \qquad (13)$$

so that

$$L_{2boundary} = \frac{V_{out}(1-D)}{2I_{out}f} \quad .$$
(14)

Since the maximum value of (14) occurs at D → 0,

$$L_2 > \frac{V_{out}}{2I_{out}f}$$
(15)

will guarantee continuous conduction for L_2 for all D. Note in (14) and (15) that continuous conduction can be achieved more easily when I_{out} and f are large.

Current Ratings for Continuous Conduction Operation

Continuous current waveforms for the MOSFET, the capacitors, and the diode in continuous conduction are shown in Figure 8 on the following page. Corresponding waveforms for the inductors were shown previously in Figures 4 and 6.

Following the same formulas and reasoning used for the buck converter, conservative current ratings for components L1, L2, the MOSFET, and the diode follow.

For L1, using Figure 5,

$$I_{L1,rms,\max}^2 = I_{in}^2 + \frac{1}{12}(2I_{in})^2 = I_{in}^2\left(1 + \frac{1}{3}\right),$$

so that

$$I_{L1,rms,\max} = \frac{2}{\sqrt{3}}I_{in} \quad .$$
(16)

Similarly, for L2, using Figure 7,

$$I_{L2,rms,\max} = \frac{2}{\sqrt{3}}I_{out} \quad .$$
(17)

MOSFET

$i_{L1} + i_{L2}$

$\Delta I_1 + \Delta I_2$

$\leftarrow I_{in} + I_{out}$

DT

0

C$_1$

i_{L1}

ΔI_1

$\leftarrow I_{in}$

0

ΔI_2

$\leftarrow -I_{out}$

$-i_{L2}$

Diode

$i_{L1} + i_{L2}$

$\Delta I_1 + \Delta I_2$

$\leftarrow I_{in} + I_{out}$

0

C

$i_{L1} + i_{L2} - I_{out}$

$\Delta I_1 + \Delta I_2$

$\leftarrow I_{in}$

0
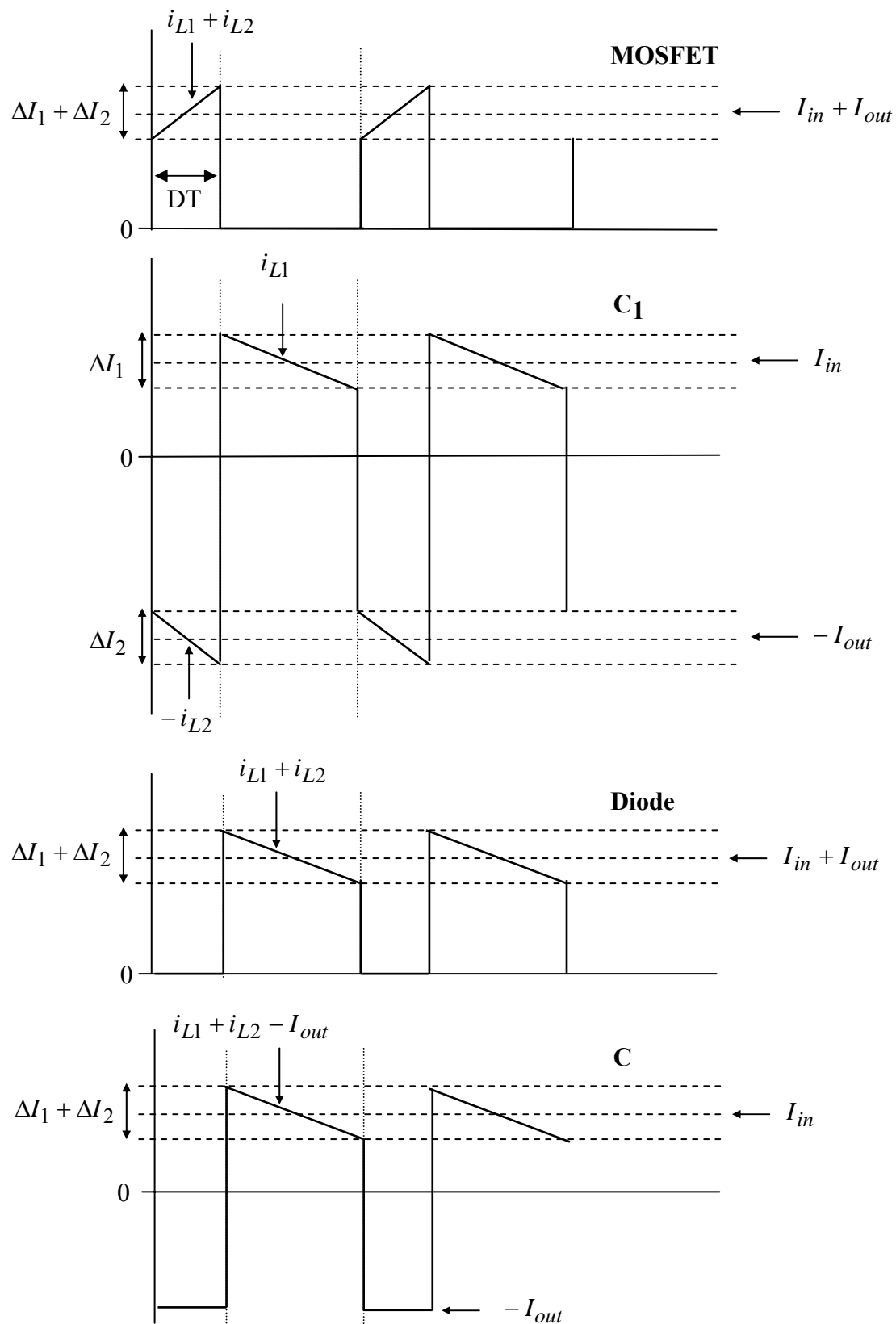
$\leftarrow -I_{out}$

Figure 8. Current Waveforms for MOSFET, Capacitors, and Diode in Continuous Conduction

For the MOSFET and diode, assuming large worst-case D, and using Figure 8,

$$I_{MOSFET,rms,\max} = \frac{2}{\sqrt{3}}\left(I_{in} + I_{out}\right) , \tag{18}$$

$$I_{Diode,rms,\max} = \frac{2}{\sqrt{3}}\left(I_{in} + I_{out}\right) . \tag{19}$$

For C1 and C, using Figure 8,

$$I_{C1,rms,\max} = \frac{2}{\sqrt{3}}I_{in} \text{ or } \frac{2}{\sqrt{3}}I_{out} \text{ , whichever is larger.} \tag{20}$$

$$I_{C,rms,\max} = \frac{2}{\sqrt{3}}I_{in} \text{ or } I_{out} \text{ , whichever is larger.} \tag{21}$$

Voltage Ratings for Continuous Conduction Operation

Referring to Figure 2b, when the MOSFET is open, it is subjected to ($V_{in} + V_{out}$). Because of the usual double-voltage switching transients, the MOSFET should therefore be rated $2(V_{in}+V_{out})$.

Referring to Figure 2a, when the MOSFET is closed, the diode is subjected to ($V_{in} + V_{out}$). The diode should be rated at $2(V_{in}+V_{out})$.

Note – "stiff" voltages across capacitors C1 and C will help hold down overshoots on the MOSFET and diode in this circuit.

Output Capacitor Voltage Ripple

The maximum ripple voltage calculation for output capacitor C follows from Figure 8 and is the same as for the boost converter, namely

$$\Delta V = \left|\frac{\Delta Q}{C}\right| = \frac{I_{out}DT}{C} = \frac{I_{out}D}{Cf} .$$

The maximum peak-to-peak ripple thus occurs as $D \rightarrow 1$ and is

$$\Delta V_{\max} = \frac{I_{out}}{Cf} . \tag{22}$$

Comparing the current graphs for C_1 and C in Figure 8 during the DT "switch closed" period, it can be seen graphically that the ripple voltage on C_1 and C are the same, i.e. Equation (22).

The Experiment
Important – to avoid excessive output voltages, always keep a load attached to the converter when it is operating. Do not exceed 90V on the converter output.

1.   Reconfigure the buck or boost components according to Figure 1 in this document.
        Secure new components C_1 and L_2. Make all connections. Capacitor C_1 is bipolar (i.e., not polarized).

2.   Connect the MOSFET Firing Circuit to your converter, **using short leads**. The firing circuit is the same as for the Boost Converter. Double check your range of D.

3.   Before connecting power, **make sure that a 5Ω ceramic power resistor is connected as a load.** View V_{GS} on Channel #1, adjust D to the minimum setting, and F to approximately 100kHz. Connect Channel #2 to view V_{DS}. Set the trigger for Channel #1.

Important Note: the first time you energize your converter, feed the 120/25V transformer through a variac, so that you can SLOWLY increase the voltage from zero and read the variac ammeter to detect short circuits before they become serious. A common problem is to have the MOSFET in backward, so that its internal antiparallel diode creates a short circuit. The ammeter on the variac is an excellent diagnostic tool. Once you are convinced that your circuit is working correctly, the variac is then optional. **Remember – your boost converter requires DC input power from a DBR.**

Does your circuit have a short? If so, do the following:

1. Make sure that your MOSFET is not connected backwards.
2. Observe V_{GS} on the MOSFET as you vary D and F. Does the waveform look correct?
3. Unplug the wall wart. Does the short circuit go away? If not, your MOSFET may be shorted – so, disconnect the MOSFET from the converter, and perform the voltage-controlled resistance test on the MOSFET.

---

4.   Connect a $25V_{ac}$ transformer to a DBR. Connect the DBR to your buck/boost converter, **keeping the wires short (i.e., 3" or less)**. Then, use a variac to energize the $25V_{ac}$ transformer and DBR. Raise the variac until V_{ac} of the transformer is approximately 27-28V.

5.   **Use a 5Ω ceramic power resistor as a load.** With **F ≈ 100kHz**, slowly increase D from its smallest value to obtain **V_{out} = 10, 20** (within ±2V), while recording D, V_{in}, V_{out}, I_{in}, I_{out}. Note by viewing V_{DS} whether or not the circuit is in continuous current operation. **For the 20V** condition, compute input and output powers and efficiency. **Do not go above 20V with the 5Ω load.**

6.   **Use a 10Ω ceramic power resistor as a load.** Turn off the DBR, and connect the 10Ω ceramic power resistor as a load. Continue the experiment as before, adjusting D, and taking D, V_{in} , V_{out}, I_{in} , I_{out} readings with **V_{out} = 30, 40V**. **Do not go above 40V with the 10Ω load.**

7.   **Use a 150W light bulb as a load.** Turn off the DBR, and connect the 150W light bulb. Continue the experiment, adjusting D, taking D, V_{in} , V_{out}, I_{in} , I_{out} readings with **V_{out} = 50, 60, 70, 80, 90V**. For the 90V case, save a screen snapshot of V_{DS} that shows the peak value.

8.   For your report, compute converter efficiencies for the **20V, 40V, and 90V** conditions. Also, plot actual and theoretical V_{out}/V_{in} versus D on one graph.

The following steps are to be performed with solar panels as the power source and with good sun (i.e., panel short circuit current of 3.5A or more). The panel voltage that you measure should be "at the panel" (i.e., the left-most analog voltmeter)

9.   Note the sky conditions. Connect a solar panel pair directly to a 150W light bulb. Measure panel voltage, panel current, and compute solar panel output power.

10.   Next, insert the buck/boost converter between the panel pair and 150W light bulb. With F ≈ 100kHz, sweep D over its range to measure and plot the I-V and P-V characteristics of the panel pair. Record the maximum power value.

Parts List
- Series capacitor, Xicon 33μF, 50V, high-frequency bipolar (i.e., not polarized), rated 14A peak-to-peak ripple current (Mouser #140-BPHR50V33)
- Second inductor like the one in the buck converter
- Second heat sink like the one in the buck converter
- Second nylon screw and lock nut like the one in the buck converter
- Two additional, 2-terminal, 30A terminal blocks (these may not be needed by students who are building minimum footprint circuits)
- 8" nylon cable tie (in student parts bin)

Appendix

Worst-Case Component Ratings Comparisons for DC-DC Converters

Converter Type	Input Inductor Current (Arms)	Output Capacitor Voltage	Output Capacitor Current (Arms)	Diode and MOSFET Voltage	Diode and MOSFET Current (Arms)
Buck	$\dfrac{2}{\sqrt{3}}I_{out}$	$1.5V_{out}$	$\dfrac{1}{\sqrt{3}}I_{out}$	$2V_{in}$	$\dfrac{2}{\sqrt{3}}I_{out}$
Boost	$\dfrac{2}{\sqrt{3}}I_{in}$	$1.5V_{out}$	I_{out}	$2V_{out}$	$\dfrac{2}{\sqrt{3}}I_{in}$
Buck/Boost	$\dfrac{2}{\sqrt{3}}I_{in}$	$1.5V_{out}$	$\max\left(\dfrac{2}{\sqrt{3}}I_{in}, I_{out}\right)$	$2(V_{in}+V_{out})$	$\dfrac{2}{\sqrt{3}}(I_{in}+I_{out})$

Additional Components for Buck/Boost Converter

Series Capacitor Voltage	Series Capacitor (C_1) Current (Arms)	Series Capacitor (C_1) Ripple Voltage (peak-to-peak)	Second Inductor (L_2) Current (Arms)
$1.5V_{in}$	$\max\left(\dfrac{2}{\sqrt{3}}I_{in}, \dfrac{2}{\sqrt{3}}I_{out}\right)$	$\dfrac{I_{out}}{C_1 f}$	$\dfrac{2}{\sqrt{3}}I_{out}$

Comparisons of Output Capacitor Ripple Voltage

Converter Type	Volts (peak-to-peak)
Buck	$\dfrac{I_{out}}{4Cf}$
Boost	$\dfrac{I_{out}}{Cf}$
Buck/Boost	$\dfrac{I_{out}}{Cf}$

Minimum Inductance Values Needed to Guarantee Continuous Current

Converter Type	For Continuous Current in the Input Inductor	For Continuous Current in L2
Buck	$L > \dfrac{V_{out}}{2I_{out}f}$	–
Boost	$L > \dfrac{V_{in}}{2I_{in}f}$	–
Buck/Boost	$L_1 > \dfrac{V_{in}}{2I_{in}f}$	$L_2 > \dfrac{V_{out}}{2I_{out}f}$

EE462L, Power Electronics, PI Controller for DC-DC Boost Converter
Version Oct. 26, 2010

Overview

In this lab, you will add feedback to your buck/boost converter. The controller will hold the output voltage at a set point by automatically adjusting the duty cycle control signal to the MOSFET firing circuit.

Introduction

A proportional-integral controller (i.e., PI) with feedback can take the place of manual adjustment of the switching duty cycle to a DC-DC converter and act much more quickly than is possible "by hand." Consider the Transformer, DBR, MOSFET Firing Circuit, DC-DC Converter, and Load as "a process" shown below. In the open loop mode that you used last time, you manually adjusted duty cycle voltage Dcont.

Dcont (0-3.5V) → Transformer, DBR, MOSFET Firing Circuit, DC-DC Converter, and Load → V_{out} (0-120V)
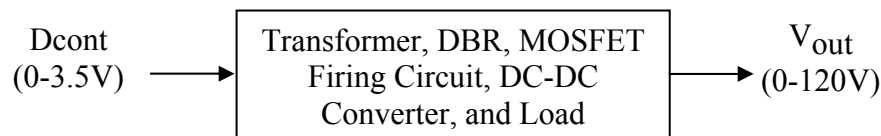
Figure 1. Open Loop Process

To automate the process, the "feedback loop" is closed and an error signal (+ or −) is obtained. The PI controller acts upon the error with parallel proportional and integral responses in an attempt to drive the error to zero.

Let αV_{out} be a scaled down replica of V_{out}. When αV_{out} equals V_{set}, then the error is zero. A resistor divider attached to V_{out} produces αV_{out}, which is suitably low for op-amps voltage levels.

Error   Dcont

V_{set} → ⊖ → PI controller → Transformer, DBR, MOSFET Firing Circuit, DC-DC Converter, and Load → αV_{out} (100V scaled down to about 1.5V)
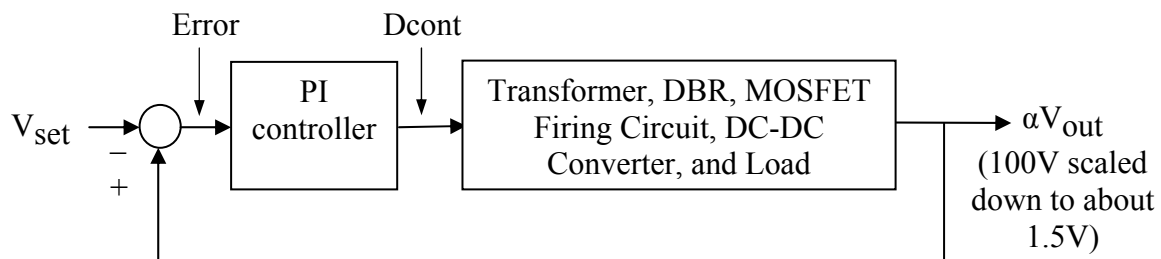
Figure 2. Closed Loop Process with PI Controller

The Circuit

A detailed circuit layout of the PI controller is given in Figure 3. A total of six op-amps are used – two as buffer amplifiers, one for error, one for proportional gain, one as an integrator, and one as a summer. Since the op-amp chips are duals, three op-amp chips are required to implement the PI controller. We use four to de-clutter the circuit. Left to right, op amps #1 and #2 are in one chip, op amps #3 and #4 (not used) are in one chip, op amps #5 and #6 are in one chip, and op amps #7 and #8 (not used) are in one chip. Inputs to unused op amps are grounded. Boxes link this figure to measurement locations in Figure 4.
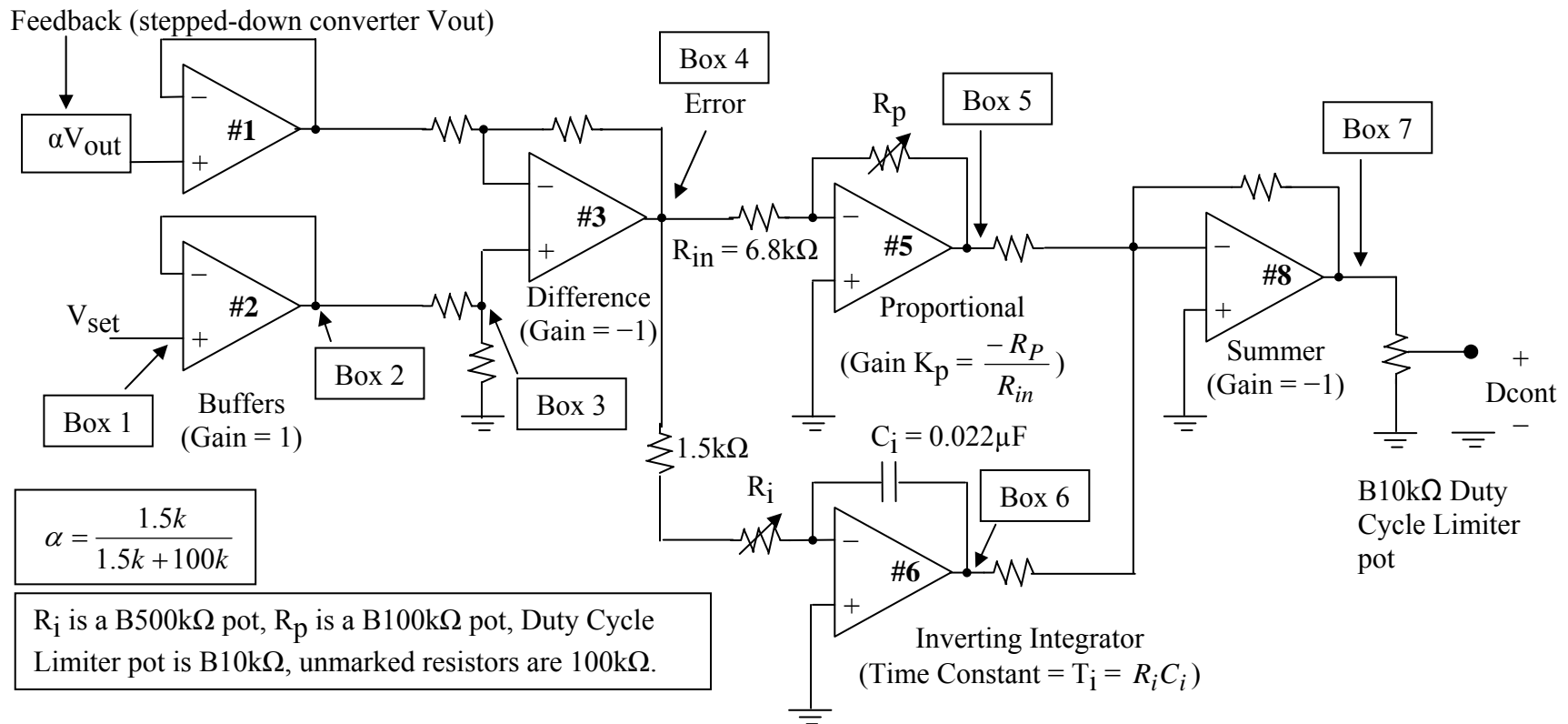
Figure 3. Op Amp Implementation of PI Controller
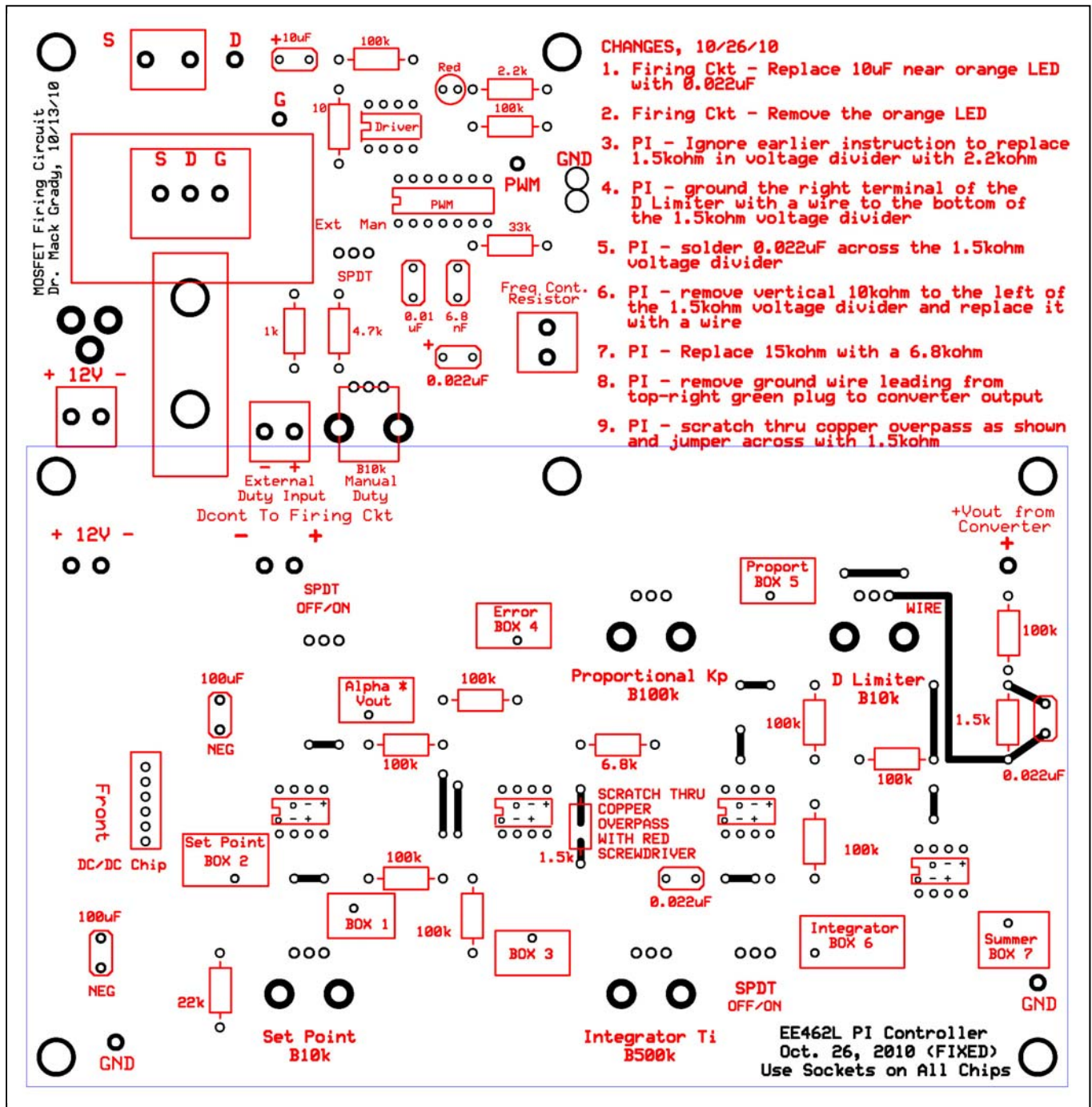
Figure 4. PC Board Implementation of PI Controller with Oct. 26 Fixes
(Bottom Layer Not Shown Here)

Obtaining Isolated ±12V from 12V Wall Wart
The op amps are powered by a 2W dual output DC-DC converter chip, 12Vdc input, isolated
±12Vdc outputs. Details for the dual output converter and its SIP socket are shown below.
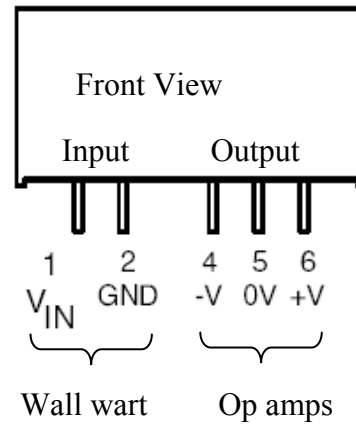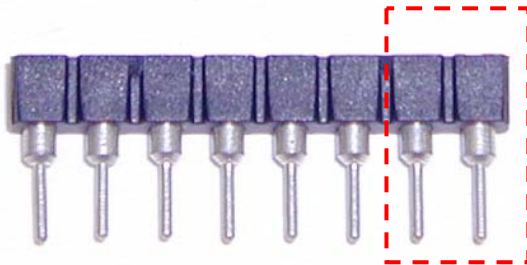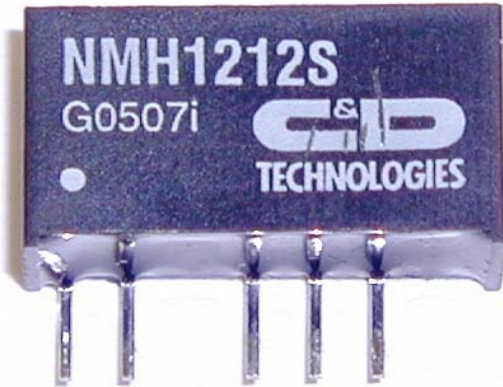
**Carefully break off two of the plastic sections
with long-nose pliers or diagonal cutters**

The Experiment

In this experiment, you will power a buck/boost converter with a DBR, and use the controller to hold regulated **100V to a 150W incandescent light bulb**. Operate your buck/boost converter at about **100kHz.**

Step 1. The PCBs
- All chips (DIP and SIP) are double-socketed. One socket is soldered to the PC board, and the other socket remains connected to the chip. Keeping chips in a socket helps preserve their leads for future use.
- Populate your PI controller. **It is very important that the 100kΩ and 1.5kΩ resistors at the top right of the board are the correct ohmic values and are properly mounted.**
- Use nylon hardware to physically connect a MOSFET firing circuit to your PI controller, overlapping as shown in Figure 4.
- For power, solder #22 red and green jumper wires from the MOSFET firing circuit 12V supply to the 12V input of the PI controller.
- Bring a #16 red wire from the output of a buck/boost converter to the PI controller terminal labeled "CONVERTER VOUT, CAREFUL, WILL EXCEED 100V."
- Use short #16 red and black wires to connect the "External Duty Input" terminal block of the MOSFET Firing Circuit to the "Dcont" terminal block of the PI controller.
- Move the SPDT switch of the MOSFET firing circuit to the left position for "External Duty Input."

Step 2. The Set Point
- **DO NOT power up the DBR in this step**.
- Rotate the **Set Point, Proportional Kp, and D Limiter potentiometers** to the **fully counterclockwise** position.
- Rotate the **Integrator potentiometer** to the **fully clockwise** position.
- **SWITCH OFF the Feedback and Integrator SPDT switches**.
- Power up the combined MOSFET Firing Circuit and PI Controller.
- Check the isolated +12V and −12V outputs on the PI controller to make sure they are OK. Voltages below 11V indicate a short circuit in your wiring, which will burn out the DC-DC chip in a few minutes.
- View V_{GS} on an oscilloscope and confirm that the waveform is clean and has a switching of about **100kHz.**
- **Raise the Set Point Potentiometer** so that the set point voltage (Box 1) is **1.5V**. This will be the "target voltage" of the controller, and it corresponds approximately to the fraction of V_{out} across the 1.5kΩ resistor when V_{out} is **100V**.
- Except for a minor tune up, the Set Point Potentiometer will remain at this value for the entire experiment. If the potentiometer knob is accidently bumped later, then simply re-adjust it as explained above.

Step 3. The D Limiter
- **DO NOT power up the DBR in this step**.
- View V_{GS} on an oscilloscope.
- **SWITCH ON the Integrator SPDT switch** to temporarily drive the integrator's output to its 12V rail.
- **Raise the D Limiter Potentiometer** so that the duty cycle of V_{GS} is approximately 0.80. The objective is to prevent the PI controller from rising to the D = 1 condition which would short circuit the MOSFET. The resulting **Dcont should be approximately 3.1V**.
- The D Limiter Potentiometer will remain at this value for the entire experiment. If the potentiometer knob is accidently bumped later, then simply re-adjust it as explained above.
- **SWITCH OFF the Integrator SPDT switch**.

Step 4. Set the Open Loop Gain to Unity
- Make sure that the **Integrator Potentiometer** is **fully clockwise**.
- Connect a 150W incandescent light bulb to the output of the buck/boost converter.
- **With a variac, 120/25V transformer, and DBR toggle switch on**, slowly raise the variac until the DBR output voltage is the usual 35-40V.
- **While viewing V_{GS}, slowly raise the Proportional K_p Potentiometer until the converter output voltage is 100V**. Re-check your DBR voltage to make sure it did not drop more than 2-3 volts. If it did, re-adjust the variac and K_p to achieve 100V output.
- The Proportional K_p potentiometer should be about mid-range. The duty cycle measurement on the scope should be about 0.65. But D will likely be jumpy and unstable, and there will probably be noticeable flicker in the light bulb. Small actions such as touching the MOSFET heat sink or measuring a voltage on the PI controller board may change the V_{GS} waveform and light brightness. These are signs of instability.
- **SWITCH OFF the DBR toggle switch.**
- Measure voltages in Box 4 and Box 5. The quotient $-V_{Box5} / V_{Box4}$ is the K_p required for unity open loop gain. We define this quotient as **KP1**. Expect KP1 to be close to $-(-10.4 / 1.52) = 6.84$.

Step 5. Perform the Open Loop Bump Test to Observe the Process Time Constant T
- Connect channel 1 probe to V_{out}.
- **SWITCH ON the DBR toggle switch**.
- Set time scale to 20msec/division, and voltage scale to 20V/division.
- Select averaging, with 1 cycle.
- Set trigger mode to normal, and adjust the trigger voltage to about 10V.
- Set trigger so that triggering occurs on positive-going change.
- Press "single" to freeze the screen on the next trigger.
- **SWITCH OFF AND BACK ON the DBR toggle switch** and capture the open loop response of the process and freeze it. **Save a screen snapshot for your report.** Upon careful examination of the saved screen snapshot, using both 20 and 5 msec/division scales on the scope, two time constants can be observed in the response. The slow one, in

Figure 5, is due to the dynamics of the transformer and DBR. The fast one, in Figure 6, is due to the dynamics of the converter itself. Two time constants are often observed when switching large capacitors in power systems and is explained by the concept of "voltage equalization" as follows: for the first few msec, the DBR capacitor and equivalent converter capacitor (reflected through the converter duty cycle switching), together with converter resistance, form a series circuit. The DBR capacitor voltage falls slightly, and the converter capacitor voltage rises significantly. Charge is conserved. The two capacitors then act in parallel with a common voltage. The dynamics of the transformer plus DBR take effect, replenishing the DBR and converter capacitors gradually.
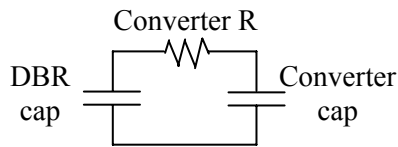
Fast time constant – voltage equalizes on two capacitors in series with the equivalent converter resistance
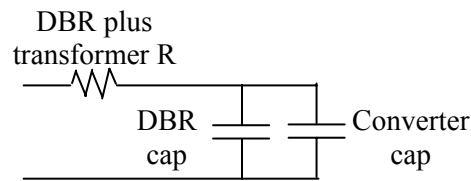
Slow time constant – two parallel capacitors, acting in series with (DBR plus transformer) resistance

- For our purposes, the DBR cap is essentially fully charged when Vout is being controlled. Thus, it is appropriate for us to use the fast time constant as our process time constant T. Estimate T from Figure 6 as the time required to rise to $\left(1 - e^{-1}\right) = 0.63$ of the asymptote. Expect T to be about 2 msec. This corresponds to the RC product of converter output capacitance (1500 to 1800 μF) and converter resistance R $= -\dfrac{\partial V}{\partial I}$ (i.e., about one ohm of Thevenin equivalent resistance).
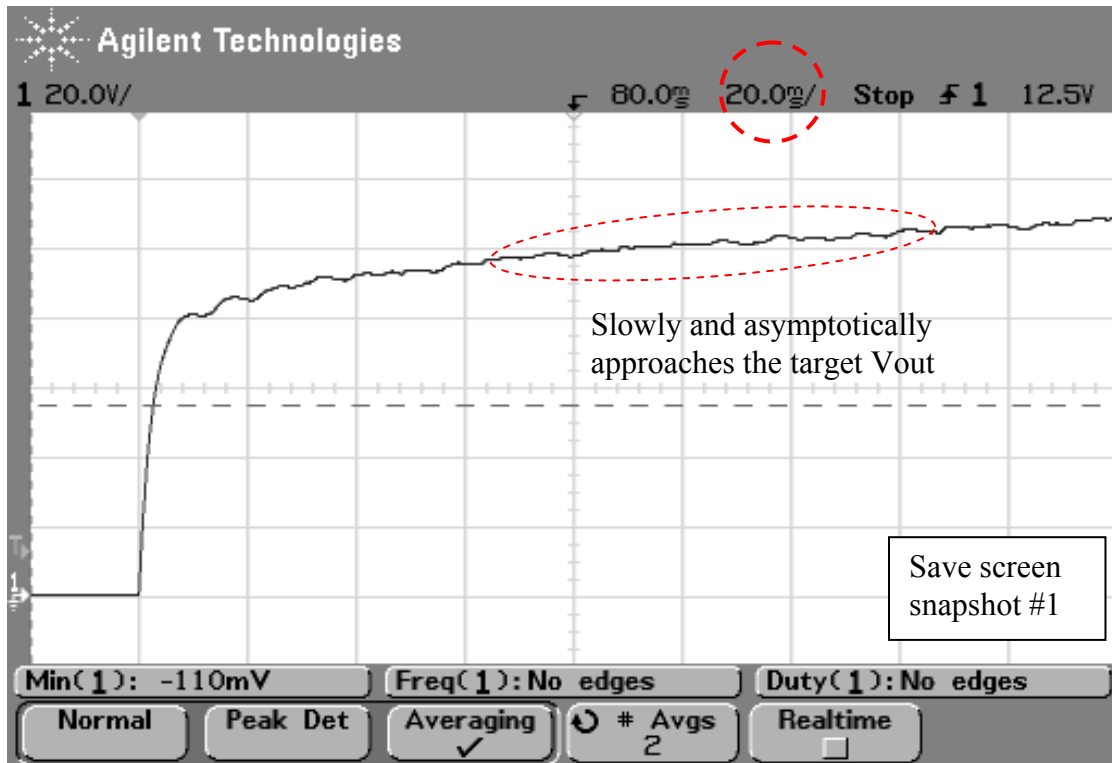
Figure 5. The Slow Time Constant of V_{out} during the Open Loop Bump Test
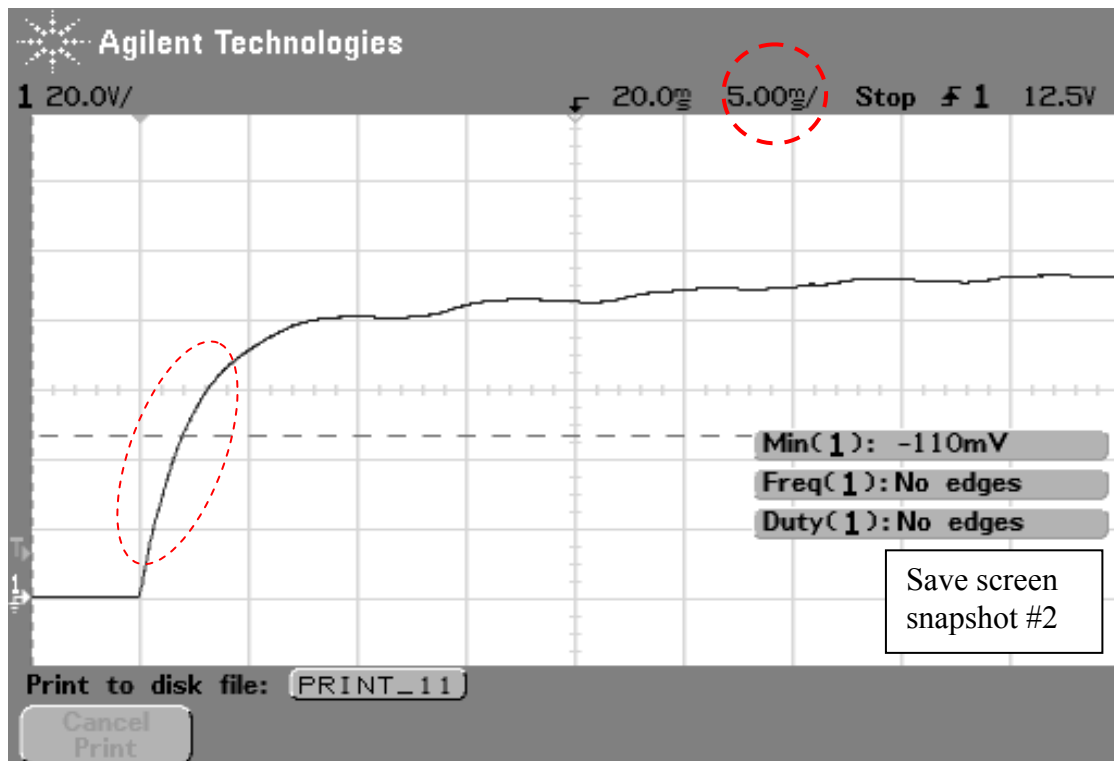
Figure 6. The Fast Time Constant of V_{out} during the Open Loop Bump Test
(this is a 5 msec/div scale zoom-in of Figure 5)

Step 6. Close the Feedback Loop and Check for Oscillation due to K_p
- With the lightbulb on, **SWITCH ON the Feedback SPDT Switch**. The light bulb will dim because the feedback voltage reduces the error signal.
- Observe and take note of the knob position of K_p. Then, sweep K_p through its range, starting from full counter-clockwise to full clockwise. If an oscillation develops, such as light bulb flicker or flicker in V_{GS}, back up on K_p until the oscillation subsides and then a bit farther. In my case, there was always oscillation, but it got much worse as I increased K_p. I settled for D ≈ 0.14 as being the approximate onset of significant oscillation, although there was no clear boundary. I was also keeping in mind the desired value of **K_p** from theory (see Appendix and the next two bullets). Remember that the theoretical equations apply to linear circuits, but our circuit is nonlinear due to the $\dfrac{V_{out}}{V_{in}} = \dfrac{D}{1-D}$ relationship. Nevertheless, the PI controller will work well.
- Measure and determine the quotient $-V_{Box5} / V_{Box4}$. We define this quotient as **KP2**. My values were $-(-4.16 / 1.30) = 3.2$.
- Compute the quotient KP2 / KP1. Gain **K_p in Appendix (A8) is the quotient KP2 / KP1**. My value was $3.2 / 6.84 = 0.47$.

Step 7. Turn on the Integrator and Carefully Sweep Integrator Time Constant T_i to Find the Boundary of Instability
- **SWITCH ON the Integrator SPDT switch**. The light bulb will immediately brighten because the controller quickly raises V_{out} to the 100V target value.
- If needed, raise the variac so that the DBR output voltage is 40V. Also, if needed, fine tune the Set Point potentiometer so that $V_{out} = 100V$.
- While watching V_{GS} on the scope, carefully lower T_i by slowly rotating the **Integrator Potentiometer counterclockwise** until signs of oscillation occur in V_{GS} and/or you detect audible buzzing. Buzzing was very noticeable in my circuit. When that happens, **SWITCH OFF the DBR toggle switch.** This is the onset of instability.
- **Turn off the 12V by unplugging the wall wart.**
- Determine R_i at the onset of instability as follows: Measure the **Integrator** potentiometer resistance by connecting an ohmmeter between the middle and right-hand prongs. Add the series 10kΩ resistor to your reading. The sum is R_i. My R_i was 20kΩ. Thus, my computed $T_i = R_i C_i = 0.44$ msec at the onset of instability. We want to stay well above this value.

Step 8. Set the Integrator Time Constant T_i

- The integrator should be faster than the process, but not so fast to create instability (such as buzzing). PI tuning rules recommend that integrator time constant $T_i = R_i C_i$ be approximately 0.8T. For our case, with T ≈ 2 msec from Step 5, and C_i = 0.022µF, then **the optimum value for R_i should be around 73kΩ**.
- Use an ohmmeter to adjust your R_i (sum of Integrator potentiometer plus 10kΩ) to the optimum value.

Step 9. Perform the Variac Test

- **Power up the PI board, and SWITCH ON the DBR toggle switch**
- While observing V_{GS}, quickly raise and lower the variac voltage. The controller should hold the light bulb brightness constant to the eye, except when the variac voltage is so low that the duty cycle limit is reached. Watch how V_{GS} changes as you turn the variac knob, and how D hits the upper limit.
- All signs of instability should have disappeared, such as when you touch the heat sink, etc.

Step 10. Perform the Closed Loop Bump Test

- Repeat the Bump Test, but this time with **Feedback and Integrator SPDT switches on**.
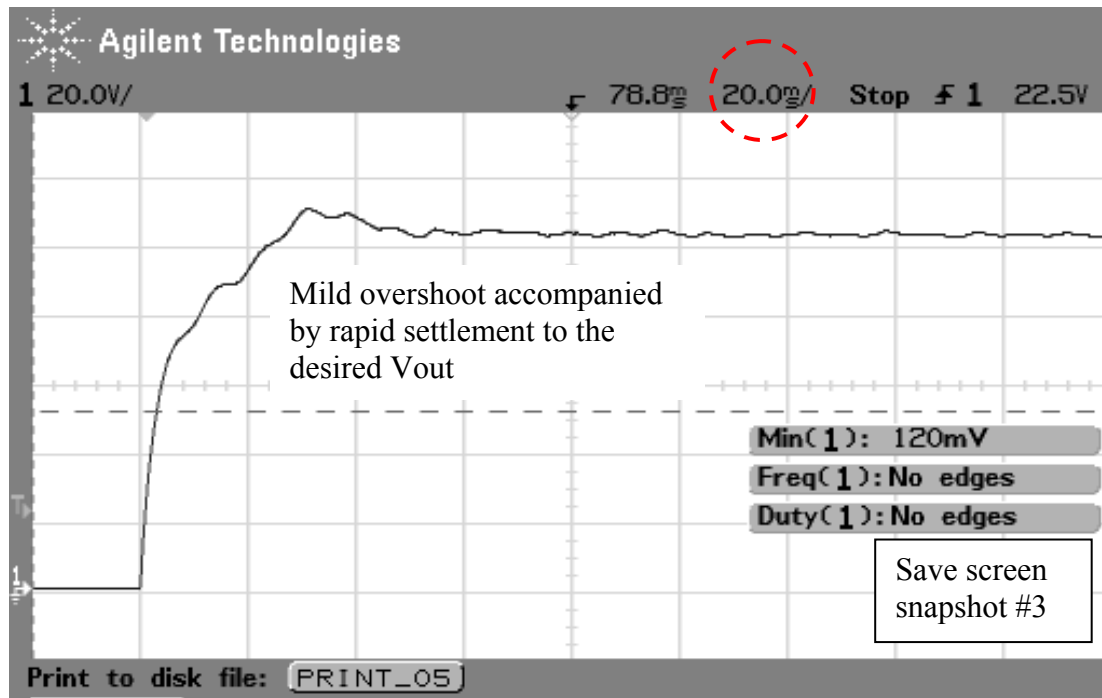
Figure 7. V_{out} during the Closed Loop Bump Test. R_i = 73kΩ, K_p = 0.47.

Step 11. Observe Sensitivity to Tuning Parameters

Observe the effect that variations in tuning parameters R_i and K_p have on bump tests.

Sluggishness indicates dominant proportional control. Too much ringing indicates dominant integral control. A proper balance is preferred. Include observations in your report.

It appears that the PI controller works well over a fairly wide range of R_i and K_p.

Example snapshots follow.

Closed Loop Bump Test, $R_i = 73k\Omega$, $K_p = 0$ (integral only)

Closed Loop Bump Test, $R_i = 73k\Omega$, K_p at the maximum

Closed Loop Bump Test, $R_i = 34k\Omega$ (just above the buzzing threshold), $K_p = 0.47$

Min(1): 1.41V
Freq(1): No edges
Duty(1): No edges

Print to disk file: [PRINT_04]
Cancel
Print

Closed Loop Bump Test, R_i at the maximum, $K_p = 0.47$ (mostly proportional)

Min(1): 120mV
Freq(1): No edges
Duty(1): No edges

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Appendix. Analysis of the Transfer Function

The circuit in Figure 2 represents the standard negative feedback block diagram with transfer function

$$\frac{V_{out}(s)}{V_{set}(s)} = \frac{G(s)}{1+G(s)H(s)}, \text{ with } H(s) = 1.$$

Thus, we have

$$\frac{V_{out}(s)}{V_{set}(s)} = \frac{G(s)}{1+G(s)}, \tag{A1}$$

where $G(s)$ is the open loop transfer function. In our case, $G(s)$ is the product of the two transfer functions

$$G(s) = G_{PI}(s) \bullet G_{TRANS+DBR+MOSFETFIRINGCIRCUIT+DCDCCONVERTER+LOAD}(s). \tag{A2}$$

The second term is the process transfer function $G_{process}(s)$. For the PI controller, the parallel proportional and integral components yield

$$G_{PI}(s) = K_P + \frac{1}{sT_i}, \tag{A3}$$

where

$$T_i = R_i C_i.$$

For the process, 1.5V input yields V_{out} (scaled) = 1.5V in steady-state, so the gain of the process here is 1.0. The converter exhibits the classic exponential rise time (i.e., charging capacitor), where C is the DC-DC output capacitor, and R is the fast Thevenin equivalent $\left(-\frac{\partial V}{\partial I}\right)$ of the process. Thus, the process transfer function is approximated with

$$G_{process}(s) = \frac{1}{1+sT}, \tag{A4}$$

where $T = RC$.

Substituting (A3) and (A4) into (A2) yields

$$G(s) = \left(K_P + \frac{1}{sT_i} \right) \bullet \frac{1}{1 + sT} \quad . \tag{A5}$$

Substituting (A5) into (A1) yields

$$\frac{V_{out}(s)}{V_{set}(s)} = \frac{\left(K_P + \dfrac{1}{sT_i} \right) \bullet \dfrac{1}{1 + sT}}{1 + \left(K_P + \dfrac{1}{sT_i} \right) \bullet \dfrac{1}{1 + sT}} = \frac{(sT_i K_P + 1) \bullet \dfrac{1}{1 + sT}}{sT_i + (sT_i K_P + 1) \bullet \dfrac{1}{1 + sT}} = \frac{(sT_i K_P + 1)}{(1 + sT)sT_i + (sT_i K_P + 1)} \, ,$$

$$\frac{V_{out}(s)}{V_{set}(s)} = \frac{T_i K_P \left(s + \dfrac{1}{T_i K_P} \right)}{s^2 TT_i + sT_i(1 + K_p) + 1} = \frac{\dfrac{K_P}{T} \left(s + \dfrac{1}{T_i K_P} \right)}{s^2 + s\left(\dfrac{1 + K_p}{T} \right) + \dfrac{1}{TT_i}} \quad . \tag{A6}$$

The denominator is the key to the response of the circuit when "bumped" by a unit step. The denominator has the standard form

$$s^2 + 2\zeta\omega_n s + \omega_n^2 \quad .$$

In our case,

$$\omega_n^2 = \frac{1}{TT_i} \quad , \tag{A7}$$

$$2\zeta\omega_n = \frac{1 + K_p}{T} \quad .$$

Solving for K_p yields

$$K_p = 2\zeta\omega_n T - 1 = \frac{2\zeta T}{\sqrt{TT_i}} - 1 = 2\zeta\sqrt{\frac{T}{T_i}} - 1 \quad . \tag{A8}$$

PI tuning procedures often call for T_i to be set to $0.8T$, which means that $\zeta > 0.447$ for feasible K_p.

Settings of $T_i = 0.8T$, $\zeta = 0.65$, $K_p = 0.45$ appear to work well in this application when using a DBR. Note that the 120Hz ripple is eliminated. Some fine tuning of T_i and K_p will probably be necessary in your circuit.
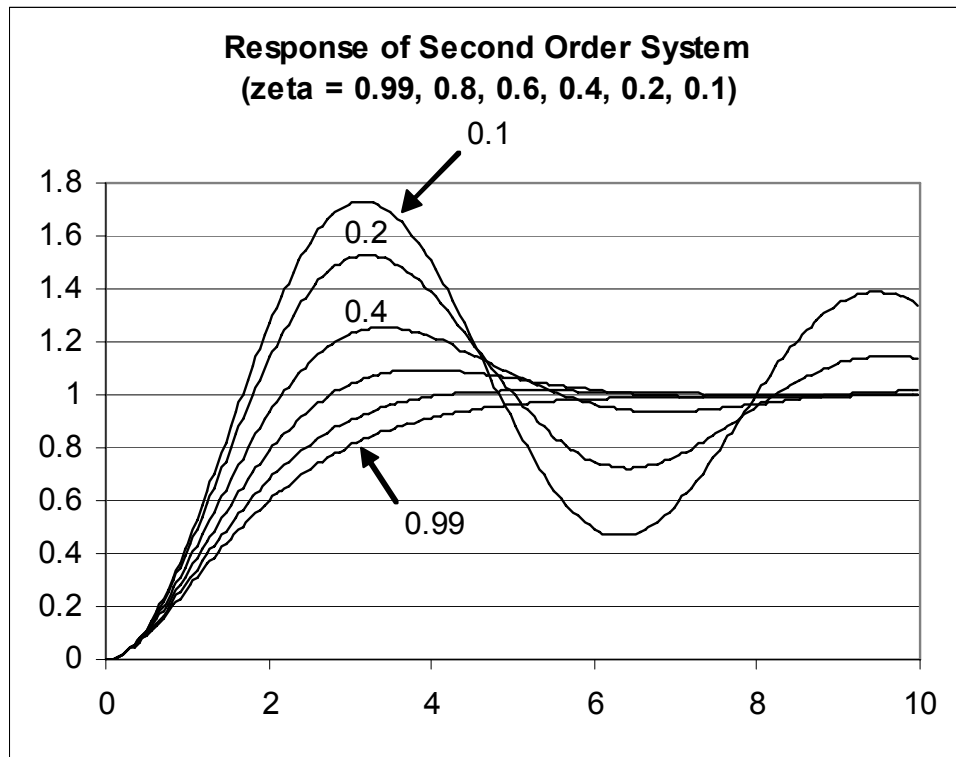
Op Amps
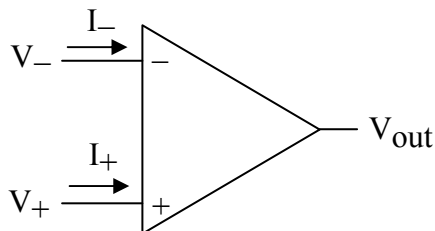
Assumptions for ideal op amp

- $V_{out} = K(V_+ - V_-)$, K large (hundreds of thousands, or one million).
- $I_+ = I_- = 0$.
- Voltages are with respect to power supply ground.
- Output current is not limited.
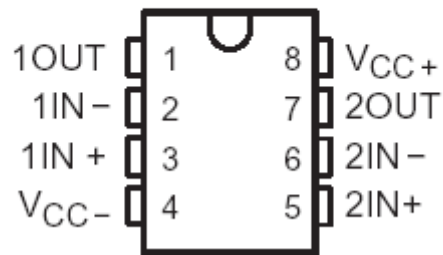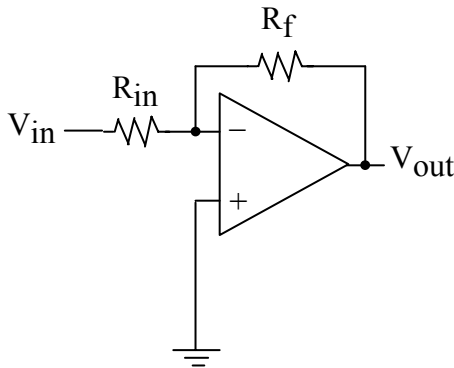
Buffer Amplifier (converts high impedance signal to low impedance signal)
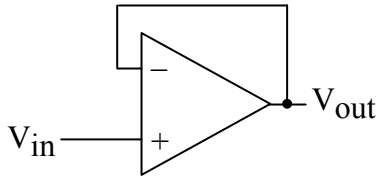
$V_{out} = K(V_{in} - V_{out})$, so $V_{out} + KV_{out} = KV_{in}$, so

$V_{out}(1 + K) = KV_{in}$, so $V_{out} = V_{in} \bullet \dfrac{K}{1+K}$. Since K is

large, then $\boxed{V_{out} = V_{in}}$.

Inverting Amplifier (used for proportional control signal)

$V_{out} = K(0 - V_-) = -KV_-$, so $V_- = -\dfrac{V_{out}}{K}$.

KCL at the − node is $\dfrac{V_- - V_{in}}{R_{in}} + \dfrac{V_- - V_{out}}{R_f} = 0$.

Eliminating V_- yields

$$\dfrac{-\dfrac{V_{out}}{K} - V_{in}}{R_{in}} + \dfrac{-\dfrac{V_{out}}{K} - V_{out}}{R_f} = 0 \text{, so}$$

$-V_{out}\left(\dfrac{1}{KR_{in}} + \dfrac{1}{KR_f} + \dfrac{1}{R_f}\right) = \dfrac{V_{in}}{R_{in}}$. For large K, then $\dfrac{-V_{out}}{R_f} = \dfrac{V_{in}}{R_{in}}$, so $\boxed{V_{out} = -V_{in}\dfrac{R_f}{R_{in}}}$.

Inverting Difference (used for error signal)
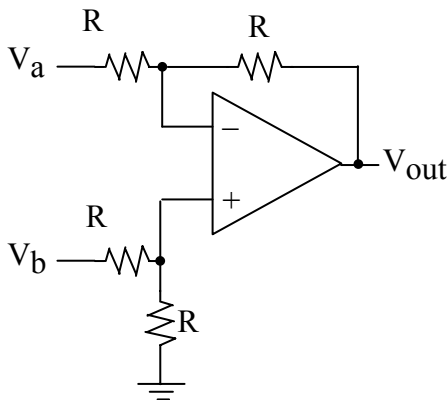
$V_{out} = K(V_+ - V_-) = K\left(\dfrac{V_b}{2} - V_-\right)$, so

$V_- = \dfrac{V_b}{2} - \dfrac{V_{out}}{K}$.

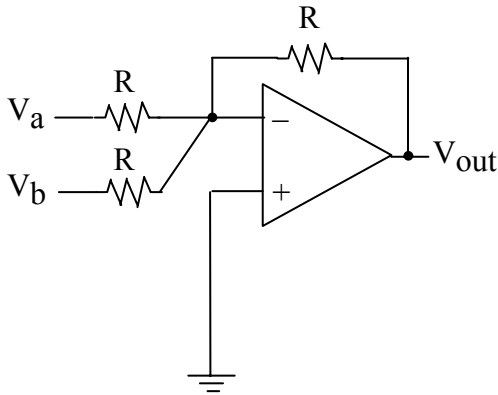KCL at the − node is $\dfrac{V_- - V_a}{R} + \dfrac{V_- - V_{out}}{R} = 0$, so

$V_- - V_a + V_- - V_{out} = 0$, yielding $V_- = \dfrac{V_a + V_{out}}{2}$.

Eliminating V_- yields

$V_{out} = K\left(\dfrac{V_b}{2} - \dfrac{V_a + V_{out}}{2}\right)$, so $V_{out} + K\dfrac{V_{out}}{2} = K\left(\dfrac{V_b - V_a}{2}\right)$, or $V_{out}\left(1 + \dfrac{K}{2}\right) = K\left(\dfrac{V_b - V_a}{2}\right)$.

For large K, then $\boxed{V_{out} = -(V_a - V_b)}$.

Inverting Sum (used to sum proportional and integral control signals)

$V_{out} = K(0 - V_-) = -KV_-$, so $V_- = \dfrac{-V_{out}}{K}$.
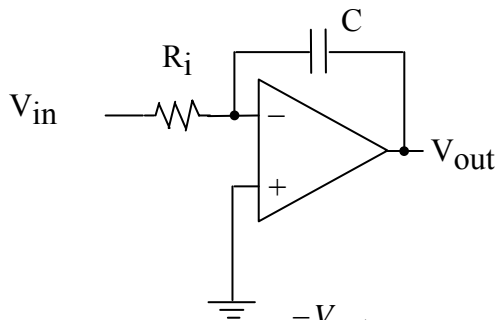
KCL at the $-$ node is

$$\frac{V_- - V_a}{R} + \frac{V_- - V_b}{R} + \frac{V_- - V_{out}}{R} = 0 \text{ , so}$$

$$3V_- = V_a + V_b + V_{out} .$$

Substituting for V_- yields $3\left(\dfrac{-V_{out}}{K}\right) = V_a + V_b + V_{out}$, so $V_{out}\left(\dfrac{-3}{K} - 1\right) = V_a + V_b$.

Thus, for large K , $\boxed{V_{out} = -(V_a + V_b)}$

Inverting Integrator (used for integral control signal)

$V_{out} = K(V_+ - V_-) = K(0 - V_-)$, so

$V_- = -\dfrac{V_{out}}{K}$. KCL at the $-$ node is

$$\frac{V_- - V_{in}}{R_i} + C\frac{d}{dt}(V_- - V_{out}) = 0 .$$

Eliminating V_- yields $\dfrac{\dfrac{-V_{out}}{K} - V_{in}}{R_i} + C\dfrac{d}{dt}\left(\dfrac{-V_{out}}{K} - V_{out}\right) = 0$. For large K,

$$-C\frac{d}{dt}V_{out} = \frac{V_{in}}{R_i} \text{ , or } \frac{d}{dt}V_{out} = \frac{-V_{in}}{R_i C} \quad . \text{ So } \boxed{V_{out} = \frac{-1}{R_i C}\int V_{in}dt.}$$

Lower R_i or C to increase integrator response.

Inverting Differentiator
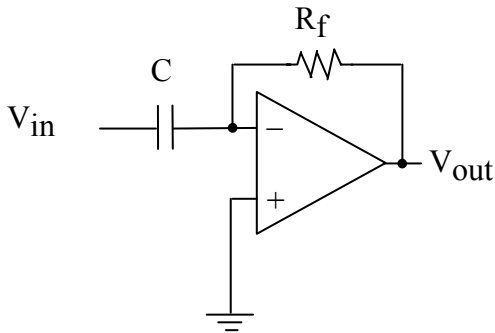
$$V_{out} = K(V_+ - V_-) = K(0 - V_-) \text{, so } V_- = -\frac{V_{out}}{K}.$$

KCL at the − node is

$$\frac{V_- - V_{out}}{R_f} + C\frac{d}{dt}(V_- - V_{in}) = 0. \text{ Eliminating } V_-$$

yields

$$\frac{\frac{-V_{out}}{K} - V_{out}}{R_f} + C\frac{d}{dt}\left(\frac{-V_{out}}{K} - V_{in}\right) = 0. \text{ For large K, we have } \frac{-V_{out}}{R_f} + C\frac{d}{dt}(-V_{in}) = 0 \text{, so}$$
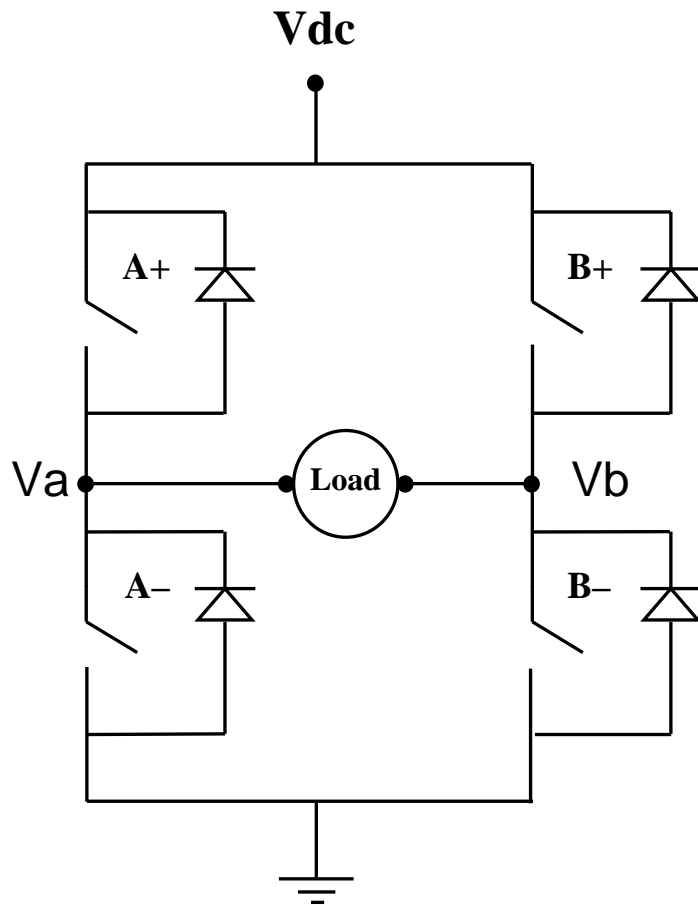
$$\boxed{V_{out} = -R_f C\frac{dV_{in}}{dt}.} \text{ Raise } R_f \text{ or } C \text{ to increase differentiator response.}$$

1. Introduction
How do we make AC from DC? Answer – the H-Bridge Inverter.

H BRIDGE INVERTER
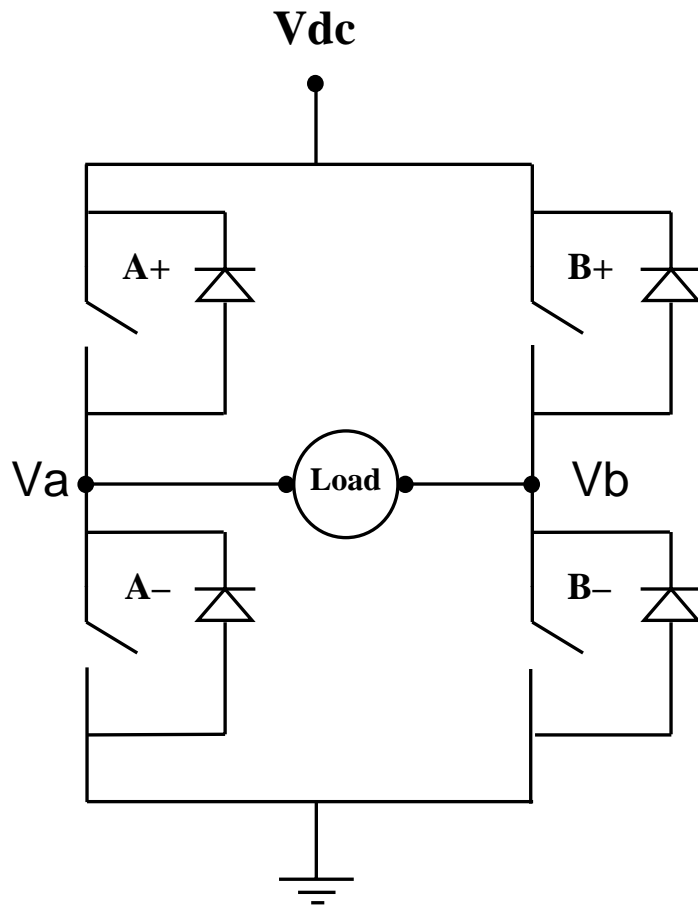
Vdc

A+

B+

Va

Load

Vb

A−

B−

Switching rules
- Either A+ or A− is always closed, but never at the same time *
- Either B+ or B− is always closed, but never at the same time *

*same time closing would cause a short circuit from Vdc to ground

Corresponding values of Va and Vb
- A+ closed, Va = Vdc
- A− closed, Va = 0
- B+ closed, Vb = Vdc
- B− closed, Vb = 0

H BRIDGE INVERTER

Vdc

Corresponding values of Vab
- A+ closed and B– closed, Vab = Vdc
- A+ closed and B+ closed, Vab = 0
- B+ closed and A– closed, Vab = –Vdc
- B– closed and A– closed, Vab = 0

A+

B+

Va

Load

Vb

- The free wheeling diodes permit current to flow even if all switches did open
- These diodes also permit lagging currents to flow in inductive loads

A–

B–

But is a square wave output good enough? Not for us! Sinusoidal load
voltage is usually the most desirable. But how do we approximate a
sinusoidal output with only three states (+Vdc, −Vdc, 0) ?
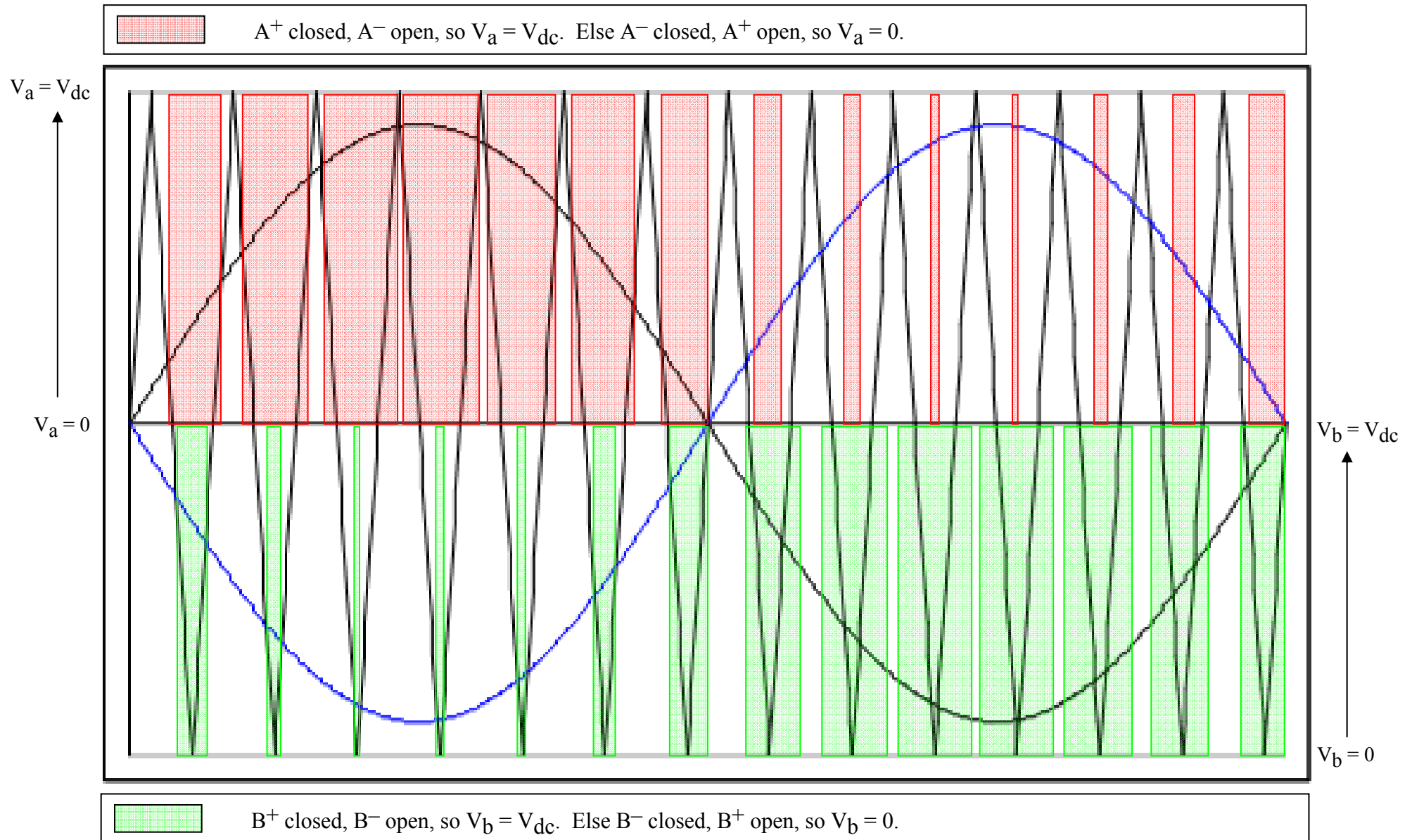The answer: Unipolar PWM modulation
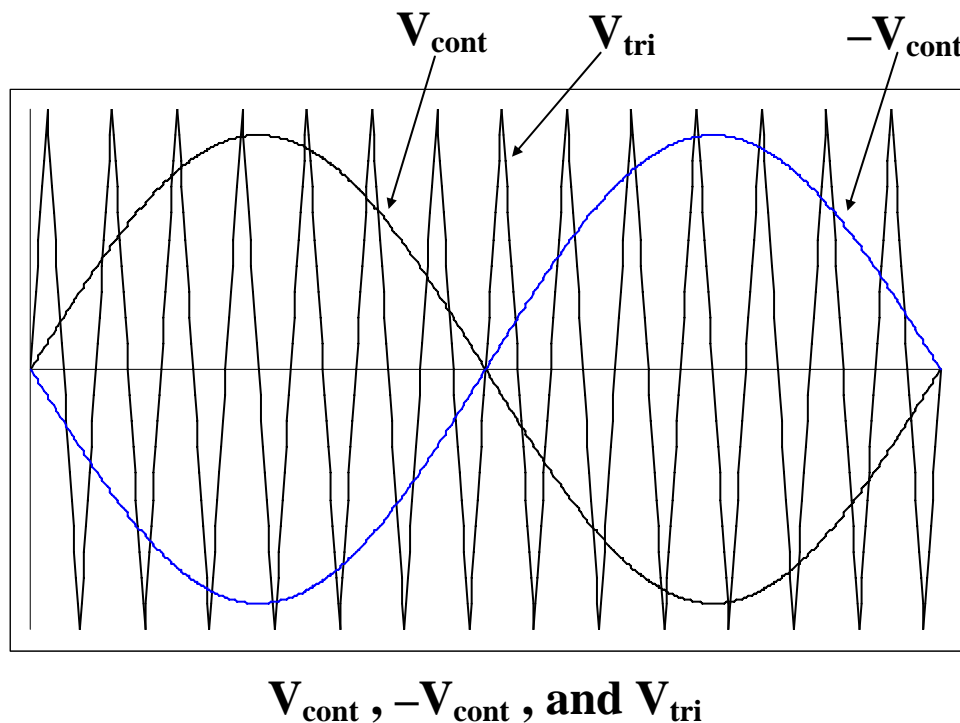
Vcont   **V**tri   −**V**cont

Vcont > Vtri , close switch A+, open
switch A− , so voltage Va = Vdc
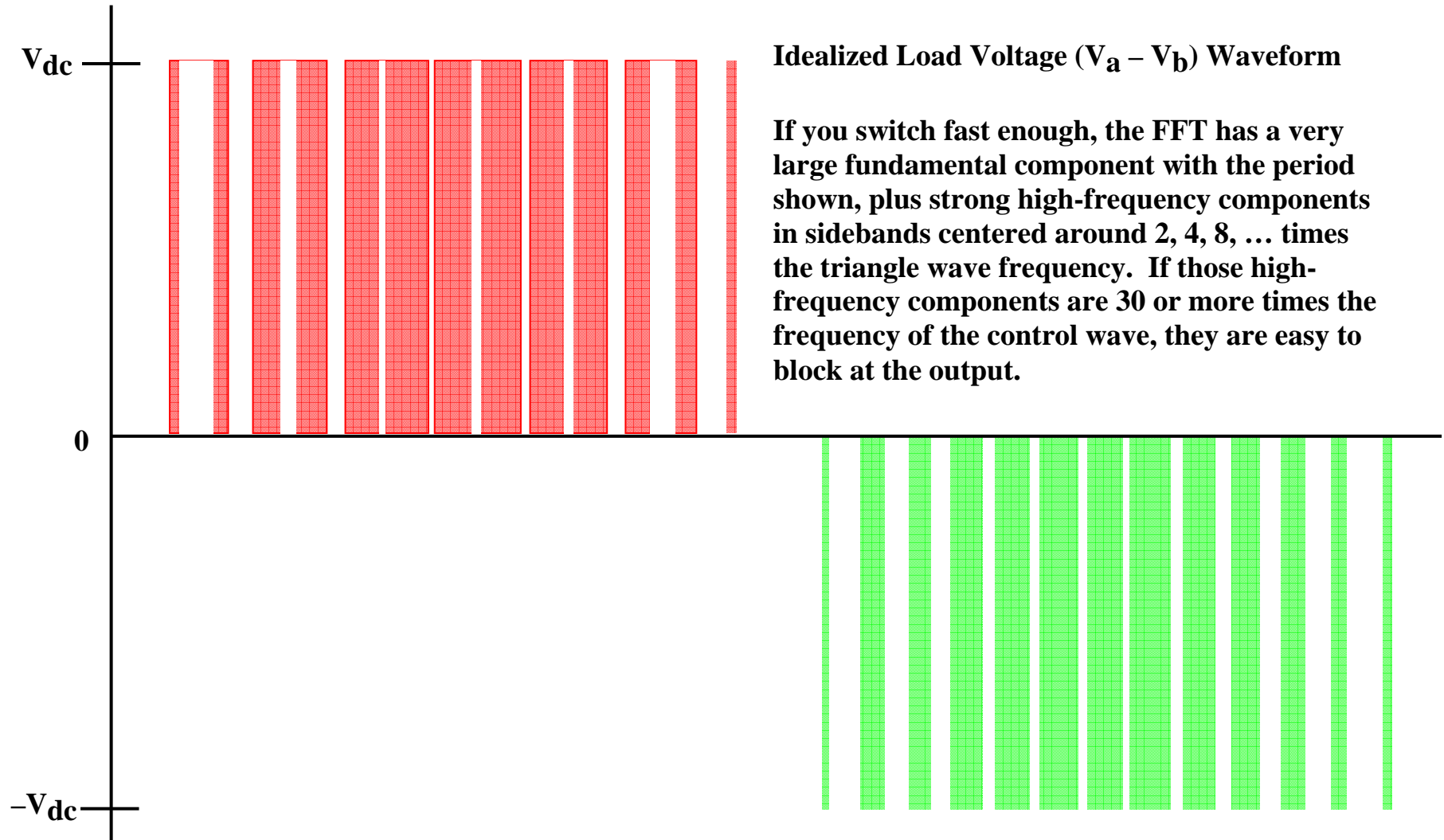
Vcont < Vtri , open switch A+, close
switch A− , so voltage Va = 0

−Vcont > Vtri , close switch B+, open
switch B− , so voltage Vb = Vdc

−Vcont < Vtri , open switch B+, close
switch B− , so voltage Vb = 0

Vcont **, −V**cont **, and V**tri

A^+ closed, A^- open, so $V_a = V_{dc}$. Else A^- closed, A^+ open, so $V_a = 0$.

$V_a = V_{dc}$

$V_a = 0$

$V_b = V_{dc}$

$V_b = 0$

B^+ closed, B^- open, so $V_b = V_{dc}$. Else B^- closed, B^+ open, so $V_b = 0$.

Idealized Load Voltage ($V_a - V_b$) Waveform

If you switch fast enough, the FFT has a very large fundamental component with the period shown, plus strong high-frequency components in sidebands centered around 2, 4, 8, … times the triangle wave frequency. If those high-frequency components are 30 or more times the frequency of the control wave, they are easy to block at the output.

Unipolar PWM inverters (also known as Class D or switching amplifiers) efficiently amplify a small input signal V_{cont}. The output voltage to the load is either $+V_{dc}$, $-V_{dc}$, or zero, depending on whether V_{cont} and $-V_{cont}$ are greater or smaller than a reference triangle wave V_{tri}. The output load voltage contains a replica of V_{cont}, and also strong harmonics centered about even multiples of m_f, where m_f is the ratio of the reference triangle wave frequency with respect to the frequency of V_{cont}, i.e, $m_f = \dfrac{f_{tri}}{f_{cont}}$.

The amplifier operates on the principle of comparing V_{cont} (and $-V_{cont}$) to a reference triangle wave V_{tri}. This principle is illustrated in Figure 1.
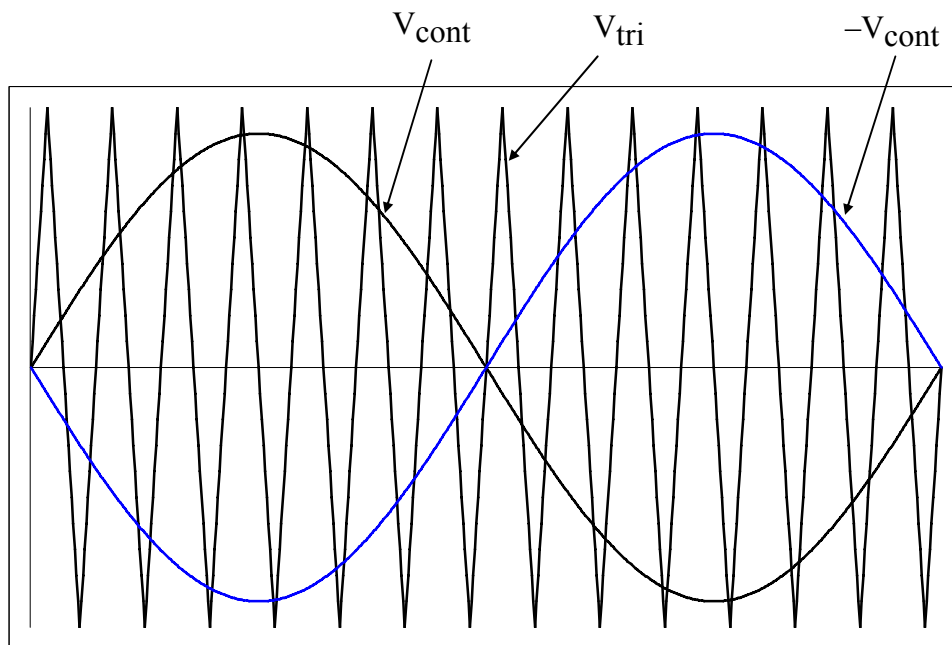

Figure 1. V_{cont}, $-V_{cont}$, and V_{tri}

The illustration given has $m_a = 0.9$, where m_a is the ratio of peak control voltage to peak triangle voltage. The logic used to operate the four switches in the H-Bridge configuration of Figure 2 is as follows:

$V_{cont} > V_{tri}$, close switch A^+, open switch A^- , so voltage $V_a = V_{dc}$

$V_{cont} < V_{tri}$, open switch A^+, close switch A^- , so voltage $V_a = 0$

$-V_{cont} > V_{tri}$, close switch B^+, open switch B^- , so voltage $V_b = V_{dc}$

$-V_{cont} < V_{tri}$, open switch B^+, close switch B^- , so voltage $V_b = 0$

30-40V$_{dc}$

A$^+$ B$^+$

Freewheeling diodes (optional in this circuit because the MOSFETS used have adequate internal reverse diodes)

a ⌁ b
$+V_{load}-$

+
V$_a$ A$^-$ B$^-$ V$_b$
+

High-frequency capacitor to provide ripple current from DC source
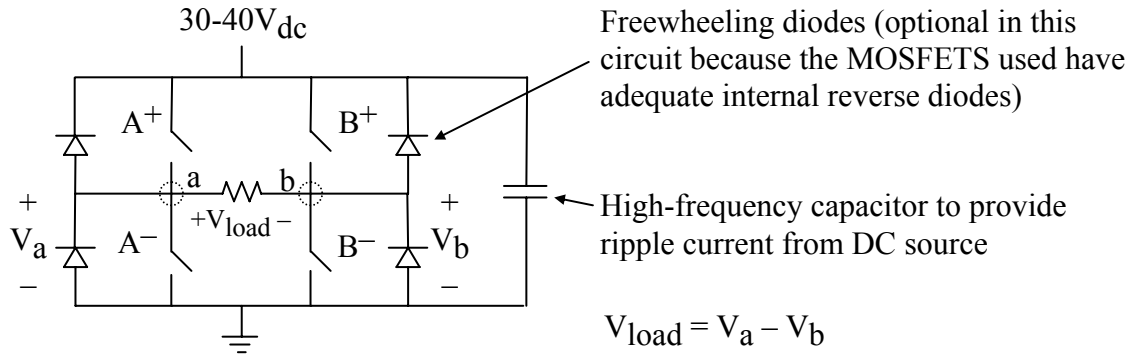
$V_{load} = V_a - V_b$

Figure 2. Four MOSFET switches configured as an H-Bridge
(note that the MOSFET source nodes are not all at the same potential, thus requiring isolated firing circuits for A$^+$ and B$^+$)

The resulting load voltage is shown in Figure 3. (Note – see the Appendix for a more complete graphical development of Figure 3). The harmonics in this waveform are high-frequency side bands $2kf_{tri} \pm f_{cont}$, $2kf_{tri} \pm 3f_{cont}$, $2kf_{tri} \pm 5f_{cont}$, and so forth, for k = 1, 2, 3, …), where f_{tri} is the frequency of the triangular wave, and f_{cont} is the frequency of V_{cont}. Waveforms for $m_a =$ 0.5 and 1.5 are shown in Figures 4 and 5.

The magnitudes of the load voltage frequency components, taken from [1], are shown in Table 1. For small m_a, many of these values are large in relation to the fundamental. However, as long as m_f is large, the undesired high frequency components are relatively easy to filter at the load, so that the output load voltage resembles V_{cont} reasonably well.
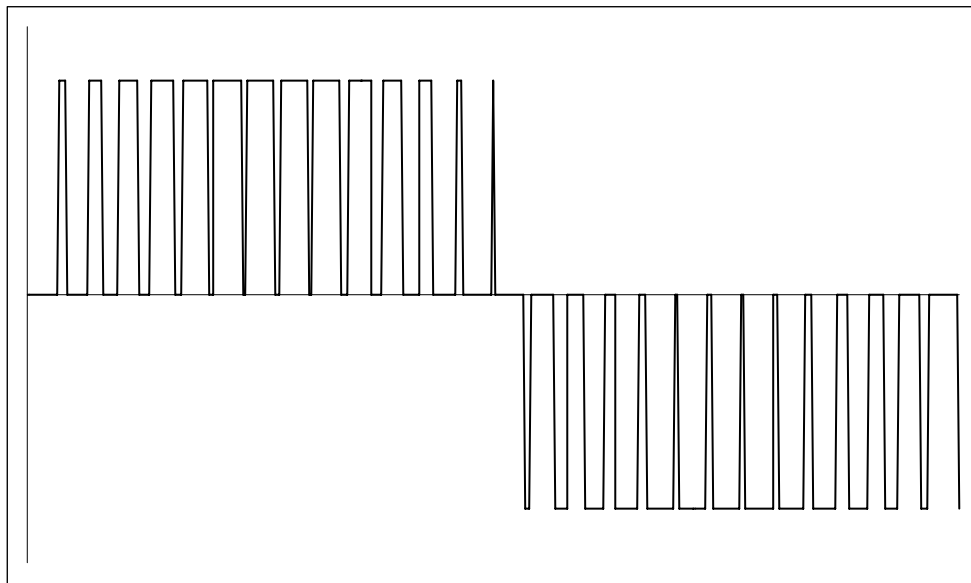

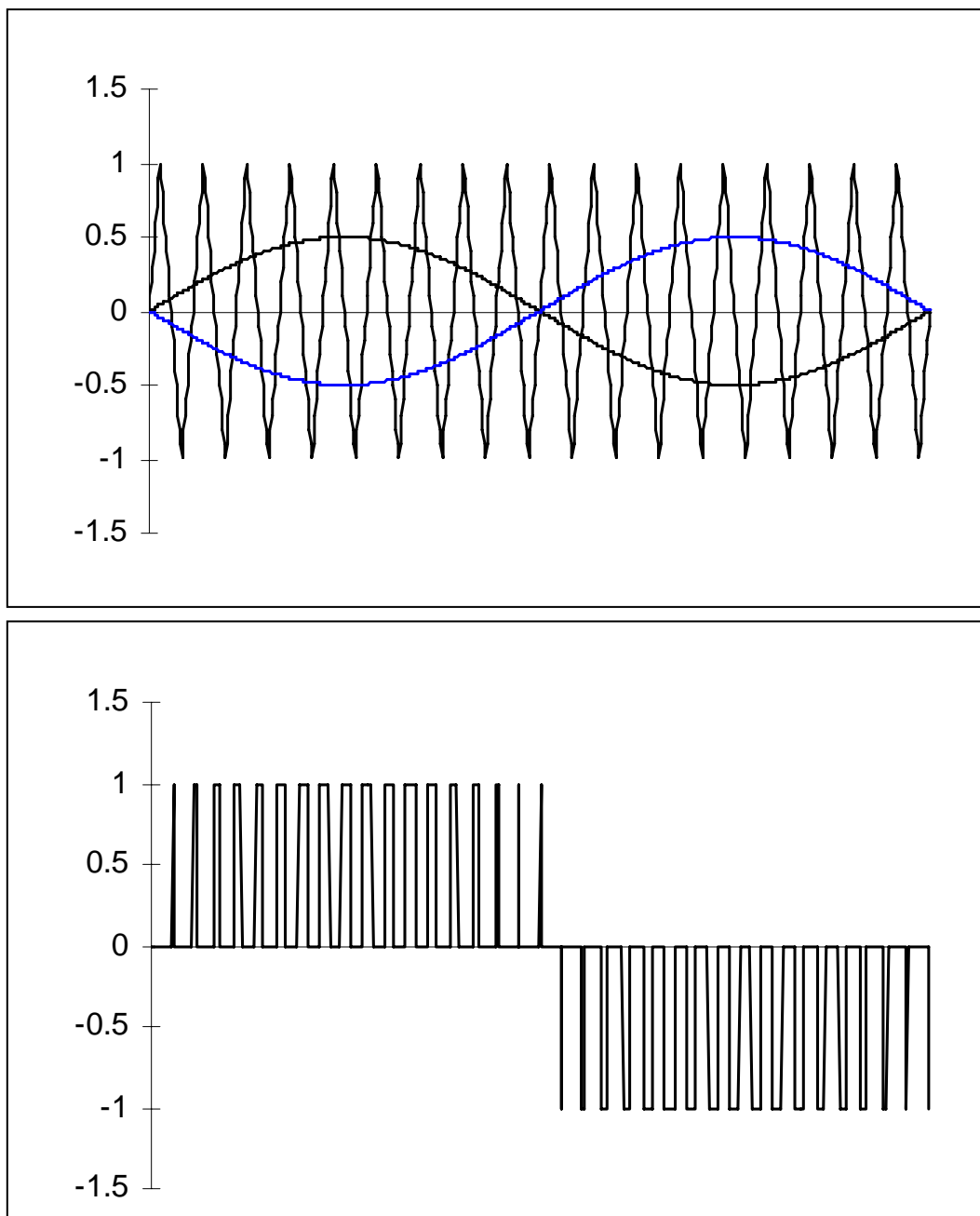Figure 3. Load voltage ($V_{load} = V_a - V_b$) with $m_a = 0.9$ (i.e., in the linear region)

Figure 4. Load voltage ($V_{load} = V_a - V_b$) with $m_a = 0.5$ (i.e., in the linear region)
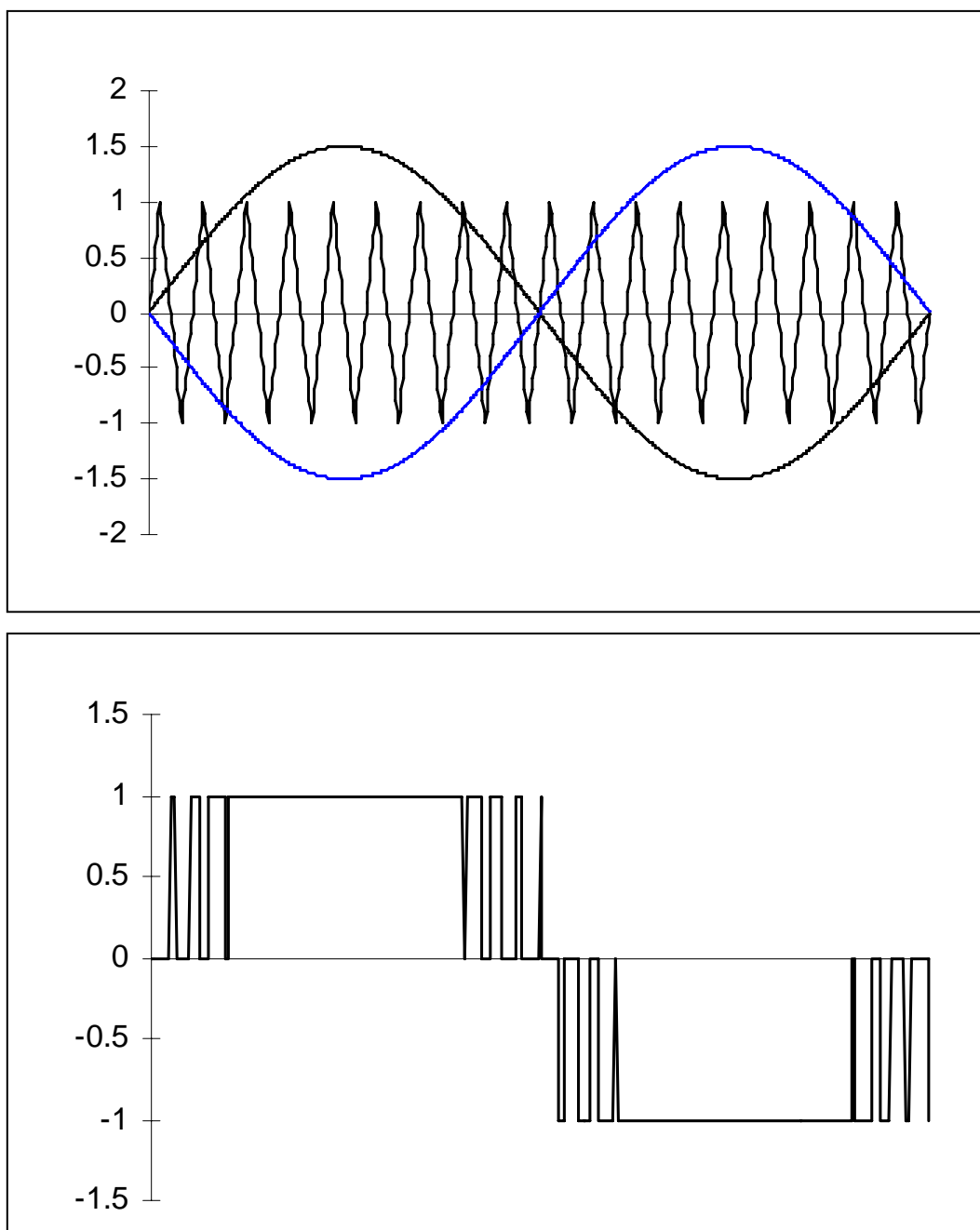
Figure 5. Load voltage ($V_{load} = V_a - V_b$) with $m_a = 1.5$ (i.e., in the overmodulation region)

Table 1. RMS magnitudes of load voltage frequency components, with respect to $\dfrac{V_{dc}}{\sqrt{2}}$

(for $f_{tri} \gg f_{cont}$)

Frequency	$m_a = 0.2$	$m_a = 0.4$	$m_a = 0.6$	$m_a = 0.8$	$m_a = 1.0$	
f_{cont}	0.200	0.400	0.600	0.800	1.000	
$2f_{tri} \pm f_{cont}$	0.190	0.326	0.370	0.314	0.181	$2f_{tri}$ cluster
$2f_{tri} \pm 3f_{cont}$		0.024	0.071	0.139	0.212	
$2f_{tri} \pm 5f_{cont}$				0.013	0.033	
$4f_{tri} \pm f_{cont}$	0.163	0.157	0.008	0.105	0.068	
$4f_{tri} \pm 3f_{cont}$	0.012	0.070	0.132	0.115	0.009	$4f_{tri}$ cluster
$4f_{tri} \pm 5f_{cont}$			0.034	0.084	0.119	
$4f_{tri} \pm 7f_{cont}$				0.017	0.050	

As m_a decreases, the on-times pulses in Figure 3 get proportionally smaller, linearly decreasing the rms value of the fundamental component of the inverter output (see Figure 4). As m_a increases beyond 1.0, then overmodulation occurs, and the on-time pulses near the centers of the output waveform gradually merge (see Figure 5). As m_a becomes very large (i.e., 5 or 10), all of the on-time pulses merge, and the inverter output becomes a square wave with predominantly low-frequency harmonics (i.e., 3rd, 5th, 7th, etc.). The variation of the rms value of the no-load fundamental output with m_a is shown in Figure 6 (taken from [1]).
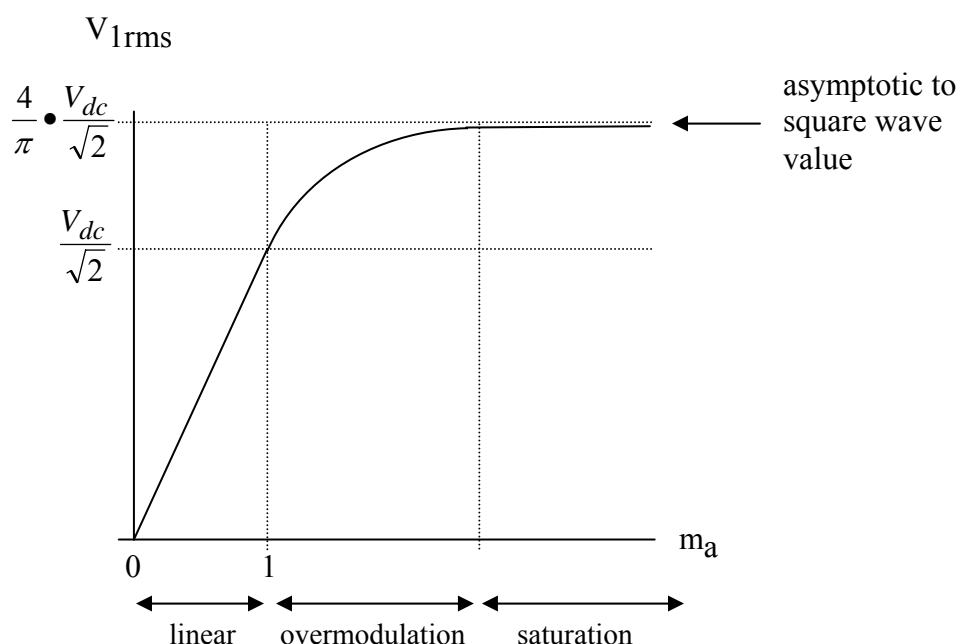

Figure 6. Variation of RMS value of no-load fundamental inverter output voltage (V_{1rms}) with m_a

In our application, V_{cont} will be a 60Hz signal taken from a benchtop waveform generator. During the tune-up procedure, Vcont will have a peak value of 4.0V (which is displayed as VPP on the waveform generator). The triangle wave will be about 150kHz.

2. The Control Circuit and Firing Logic

The PWM inverter control circuit is shown in Figure 7. The purpose of this control circuit is to produce firing signals for the four H-Bridge MOSFETs. Firing signal VA controls MOSFETs A^+ and A^-. Firing signal VB controls MOSFETs B^+ and B^-. When VA is "high," A^+ is "on" and A^- is "off." When VA is "low," A^+ is "off" and A^- is "on." The "B-side" of the H-Bridge works the same way with VB. Thus,

- node voltages V_a and V_b in Figure 2 will be working-voltage replicas of firing signals VA and VB, respectively, and
- $V_{load} = V_a - V_b$ will be a working voltage replica of [VA – VB].

The purposes of the four ICs in this circuit are

- 2W, DC-DC converter chip to produce isolated ±12V from one plug-in 12V regulated "wall wart" DC power supply. The wall 0V output of the DC converter chip will not be connected to the wall wart ground.
- One dual Op Amp – one side sums two input voltages to produce a mono signal, and the other side can attenuate or boost the mono signal.
- Another dual Op Amp with only one side used. Has adjustable gain to produce –Vcont.
- Waveform generator – generates the triangle wave. Regulated ±12Vdc input keeps the waveform steady and helps to eliminate DC in the output.
- Comparator – performs the PWM comparison logic, and sinks enough current so that the MOSFET drivers switch on-and-off properly. Because comparisons are made between voltages that can be positive or negative, the comparator chip must powered by a ± supply voltage (in our case ±12V), and the comparator chip output is either +12V, or −12V.

See the Appendix for IC pin configurations.
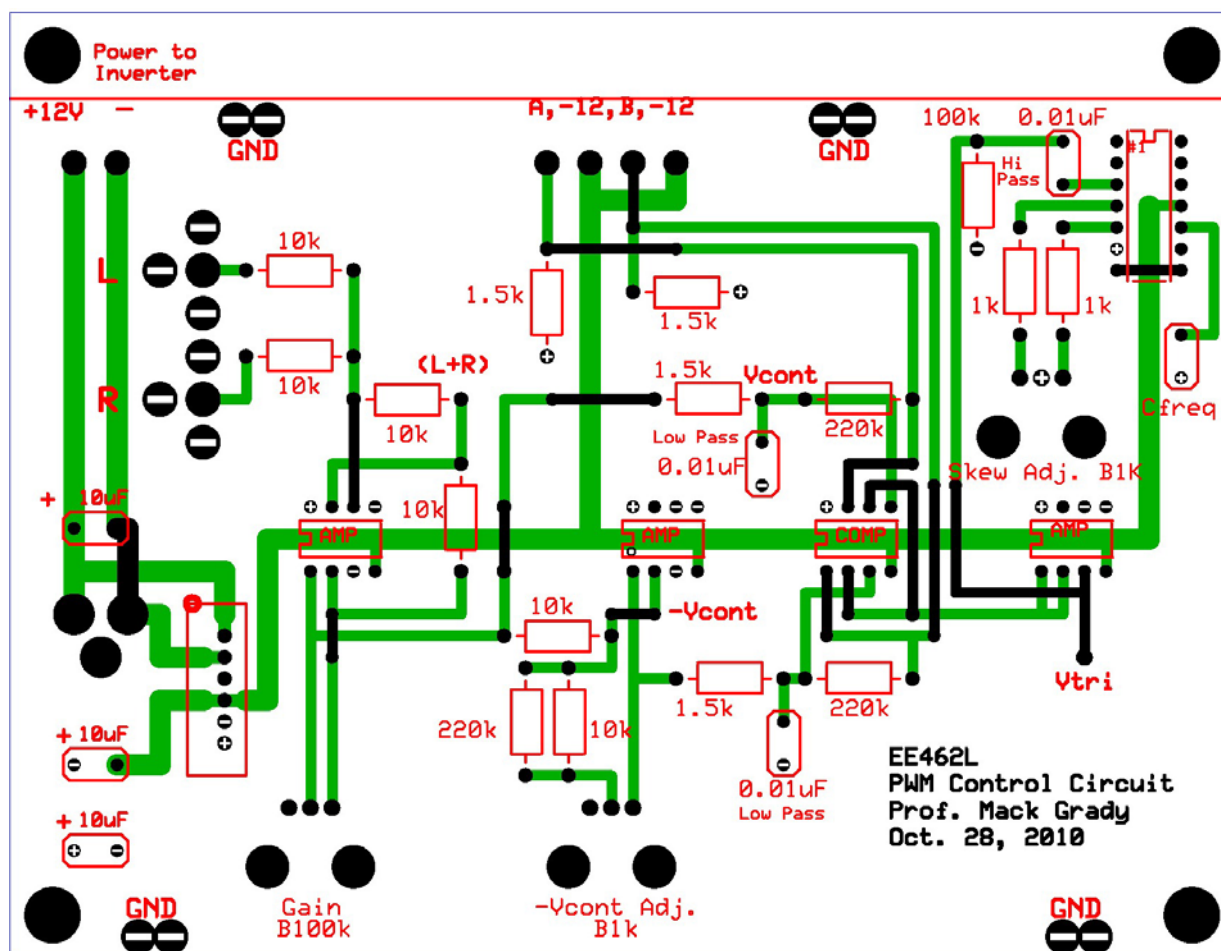
Figure 7. PWM Control Circuit

Dual Op Amp

NTE864 Precision Waveform Generator. Spec on Cfreq is
- **680pF yields 200kHz,**
- **500µF yields 0.001Hz**

Pin #	Symbol	Type	Description
1	SA1	I	Wave Form Adjust Input 1.
2	SWO	O	Sine Wave Output.
3	TWO	O	Triangle Wave Output.
4	DCA1	I	Duty Cycle Adjustment Input.
5	DCA2	I	Duty Cycle Adjustment Input.
6	V$_{CC}$		Positive Power Supply.
7	FMBI	I	Frequency Modulation Input.
8	FMSI	I	Frequency Sweep Input.
9	SQO	O	Square Wave Output.
10	TC	I	Timing Capacitor Input.
11	V$_{EE}$		Negative Power Supply.
12	SA2	I	Wave Form Adjust Input 2.
13	NC		No Connect.
14	NC		No Connect.

+12V   VA   Vtri   Vcont

Vcc   OUTPUT 2   IN2(−)   IN2(+)

8   7   6   5

If Vcont > Vtri, Then
   VA = 12V, so
   VA = 24V (w.r.t. −12V)
   Else
   VA = −12V, so
   VA = 0V (w.r.t. −12V)
Endif

1   2   3   4

OUTPUT 1   IN1(−)   IN1(+)   GND

If −Vcont > Vtri, Then
   VB = 12V, so
   VB = 24V (w.r.t. −12V)
   Else
   VB = −12V, so
   VB = 0V (w.r.t. −12V)
Endif

VB   Vtri   −Vcont   −12V

Dual Comparator

220kΩ resistors between Inputs+ and Outputs provide hysteresis to prevent rapid switching due to noise
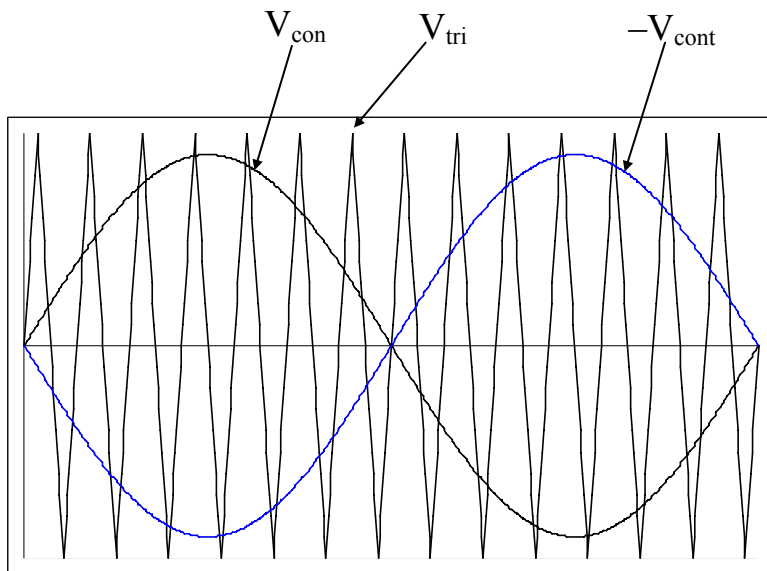
V_{con} V_{tri} $−V_{cont}$

Vcont > Vtri , close switch A+, open switch A− , so voltage Va = Vdc

Vcont < Vtri , open switch A+, close switch A− , so voltage Va = 0

−Vcont > Vtri , close switch B+, open switch B− , so voltage Vb = Vdc

−Vcont < Vtri , open switch B+, close switch B− , so voltage Vb = 0

- VA and VB outputs, relative to −12V, are produced to switch the H-bridge MOSFET driver chips. These two voltages are related to the logic on page 1 and to the circuit in Figure 7.

3. Calibration Process

Note – From now on, anytime that you use your circuit, you should always
- **Make sure that your triangle wave rise and fall times are identical**
- **Use a 60Hz, 2.5Vrms Vcont to make sure that the –Vcont gain setting is correct**
- **Re-test Figures 8 and 9 using a 60 Hz sinusoidal Vcont.**

1. Once you have populated the PC board, energize the circuit with a 12V wall wart. Do not apply a Vcont signal until later in the experiment.

2. Use a multimeter to confirm the +12V and −12V supply voltages produced by the DC-DC converter chip. Voltages below about 11.5V indicate a partial short circuit somewhere on your PC board. If that is our case, unplug and find the short circuit.

3. View the high-pass filtered output of the triangle wave generator on an oscilloscope. It should be clean, steady, around 150-200kHz (based on time between peaks), have max/mins of about ±4.2V, and have an absolute DC value less than 0.05V.

4. Adjust the skewness potentiometer until the triangle wave rise and fall times are visually the same. Then, use the scope to measure rise and fall times. The two values should be within ½ of the third significant digit of each other, or about 0.05µsec.

5. Display outputs (VA to −12V ref) and (VB to −12V ref) on a scope. The two waveforms should be sharp (except for some mild corner rounding), identical, in phase, 0 to 24V square waves, with 50% duty cycle and the same frequency as the triangle wave.

6. Use a multimeter to measure **the true RMS value** of (VA – VB). The value should be less than 50mV. When taking this measurement, it may help to remove the scope probes.

7. **Apply a 4.0V peak, 60Hz sinusoidal Vcont from the benchtop waveform generator to either left or right Vcont inputs of your circuit**. (Oddly, the waveform generator displays VPP = 4.0 when the actual voltage is 4.0V zero-to-peak.) Use a multimeter to read the **true rms value** of V(L + R). Expect 2.8Vrms.

8. Adjust your PCB gain potentiometer so that the **true rms value** of post-filtered Vcont is about 2.5Vrms. Then, **critical**, adjust the –Vcont potentiometer so that the **true rms value** of post-filtered –Vcont is within 0.01V of Vcont.

9. Simultaneously view Vcont and –Vcont on a scope. The waveforms should be clean, sinusoidal, have equal magnitudes, and be 180º out of phase.

10. Use a multimeter to measure the DC value of (VA – VB). Expect the absolute value to be 0.3V or less. Again, it may help to remove the scope probes.

11. Measure the **true rms value** of (VA – VB). Expect about 15V.

4. Waveform Checks

4.1 View unfiltered VAB. Begin the output waveform checks by attaching a scope probe across outputs A and B to view (VA – VB). **Do not use the scope filter.** Set the time scale to about 5msec/div to observe the cycles of 60Hz. When m_a is in the linear region, you will see the fuzzy waveform below. For now, pay no attention to the FFT curve also shown in the figure.
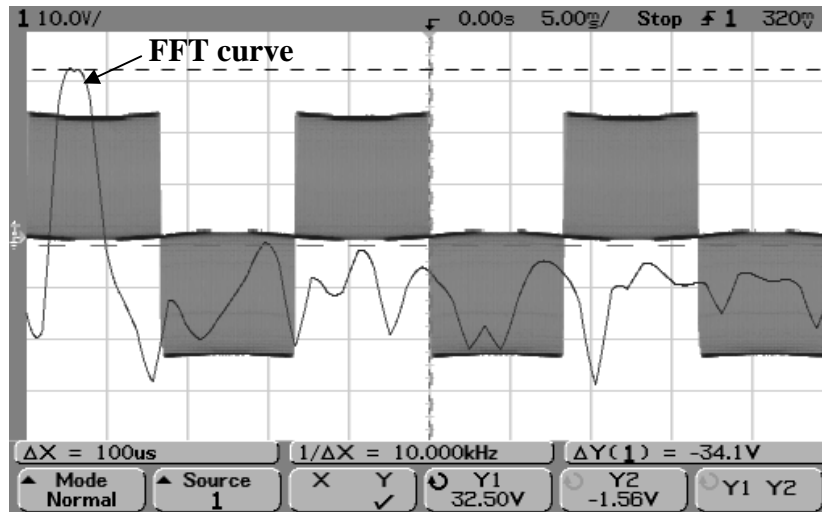

VAB for $0.9 < m_a < 1.0$ (not yet into overmodulation)

As you raise m_a into overmodulation, a split will form where Vcont is greater in magnitude of the triangle wave peak. Ideally, the splits are perfectly symmetrical.
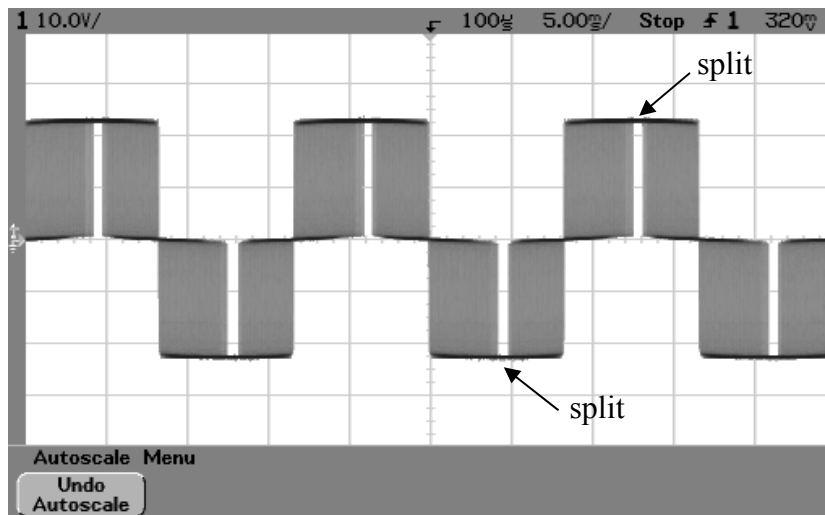

VAB for $m_a > 1$, just into the overmodulation region

Continue by making sure that your **filtered** VA-to-ground, VB-to-ground, and VA-to-VB output waveforms are correct. This means that, when viewed using the scope filter, they are sinusoidal in the linear region, and the flat topping is symmetric in the positive and negative voltage swings as you move into saturation.

4.2. Simultaneously view VA-to-ground and VB-to-ground, using the scope filtering feature. The sinusoidal waveforms should be identical in magnitude and shape except for a 180 degree shift. They should have the same average value and that value should be close to zero.
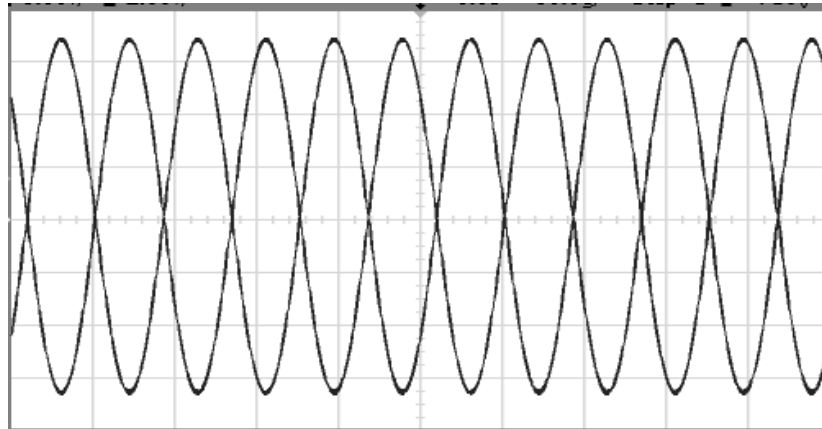
4.3. Display the FFT of VA-to-ground, using a 1kHz span centered at 500Hz (or as close as you can get to those settings). .
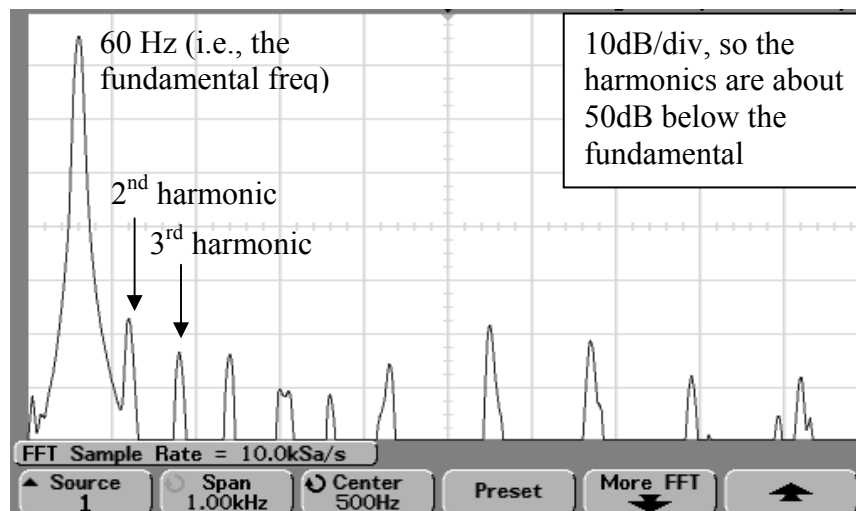
4.4. Repeat for VB-to-ground

VB-to-ground is also good
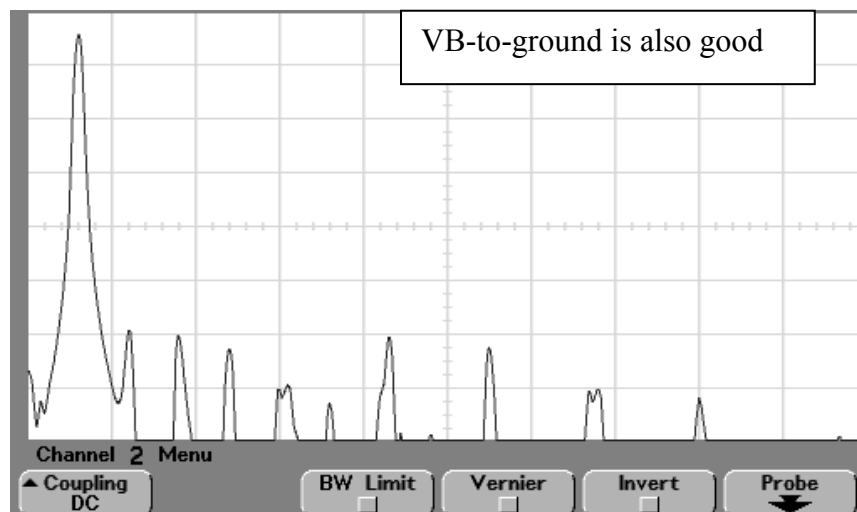
4.5. Repeat for (VA-to-VB), using the VA – VB option in the scopes FFT.
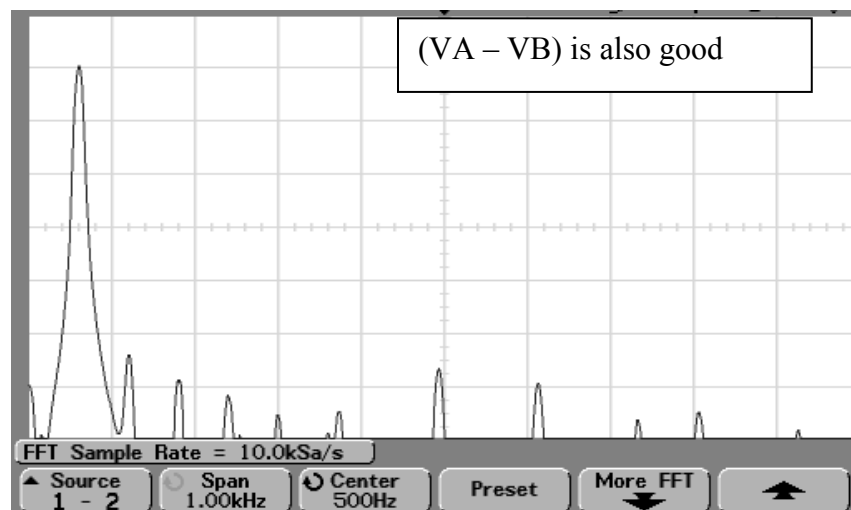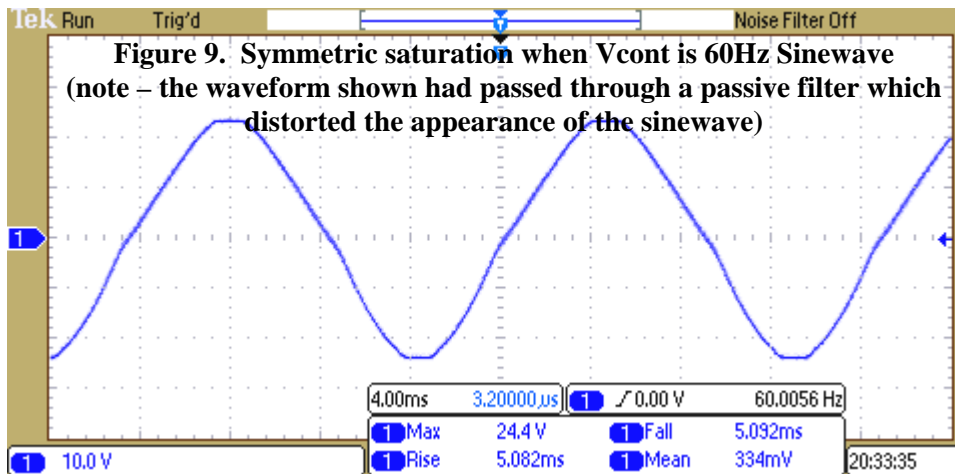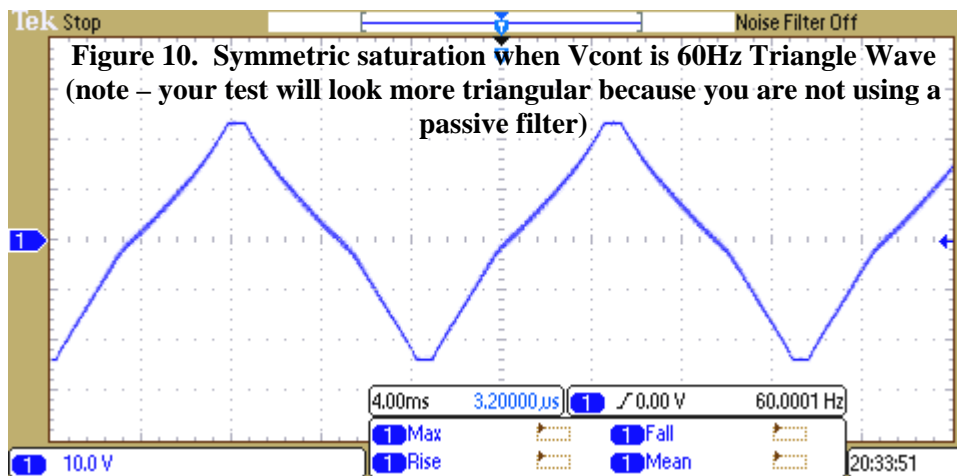

(VA – VB) is also good

Figure 8. FFT of (VA – VB) with 60Hz Vcont in Linear Region

4.6. Check symmetry in saturation. The best way to do this is to observe flat-topping at the onset of saturation. Starting with your existing sinusoidal input, slowly raise the Gain Potentiometer into saturation (i.e., $m_a > 1$ where flat-topping begins). Flat-topping should be symmetric on the positive and negative peaks of the waveform. If it is not symmetric, then it may be that your –Vcont magnitude is wrong, or that your triangle wave does not have equal rise and fall times, or perhaps has a DC value.

Figure 9. Symmetric saturation when Vcont is 60Hz Sinewave (note – the waveform shown had passed through a passive filter which distorted the appearance of the sinewave)

Save screen snapshot #1

For even finer adjustment, switch the benchtop waveform generator from sinewave to triangle wave.

Figure 10. Symmetric saturation when Vcont is 60Hz Triangle Wave (note – your test will look more triangular because you are not using a passive filter)

Save screen snapshot #2

Anytime that you use your circuit, you should re-test Figures 8 and 9.

5. Tutorial on FFT Measurements

This portion of the document has not yet been modified for the new scopes and F = 100-to-200kHz operation of the PCB station (versus 22kHz in previous semesters). However, your steps will be essentially the same as those described here. Expect FFT clusters near 2F and 4F.

1. The FFT capability of the scope is useful in determining the magnitude of the significant frequencies found in the idealized load voltage waveform. Using sinusoidal Vcont, adjust V_{cont} so that (visually) $0.90 < m_a < 1$ (i.e., just prior to the formation of the gap in Figure 11). Then, press the "math" key to use the FFT feature. Adjust the span to 100kHz, adjust the center frequency to 50kHz, and adjust the time axis until the sample rate is 200kSa/s (kilosamples per second). You should see something similar to Figure 11. Freeze and capture the oscilloscope trace. The frequencies with the largest components are easily identified. The frequency span, together with the x-axis grid (or cursors), identify their frequencies.
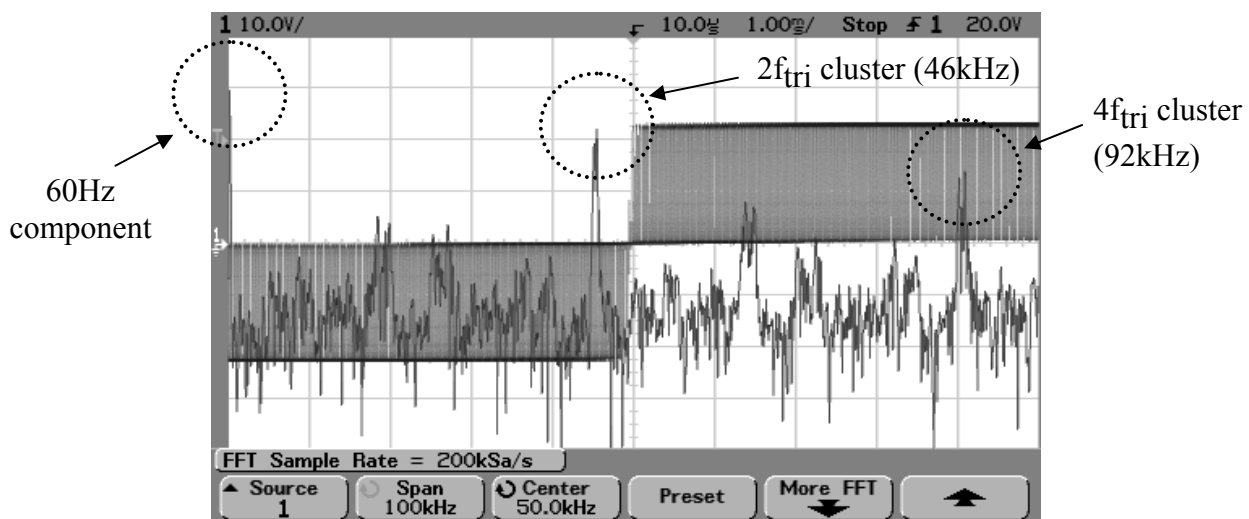

Figure 11. FFT of idealized V_{load} in the linear region with $m_a \approx 1.0$, where the frequency span and center frequency are set to 100kHz and 50kHz, respectively

By pushing "More FFT" you can observe and adjust the db scale. If the db scale is 10db/division, while the voltage scale is 10V/division, then each scale volt corresponds to 1db.

Use the cursors to measure the magnitude of the $2f_{tri}$ cluster (i.e., approx. 46kHz) with respect to the 60Hz component (in scale volts). **Save a snapshot of your waveform.** Convert your volts to db. Then compute the ratio from the $\log_{10}$ relationship. For Figure 12, the computation yields
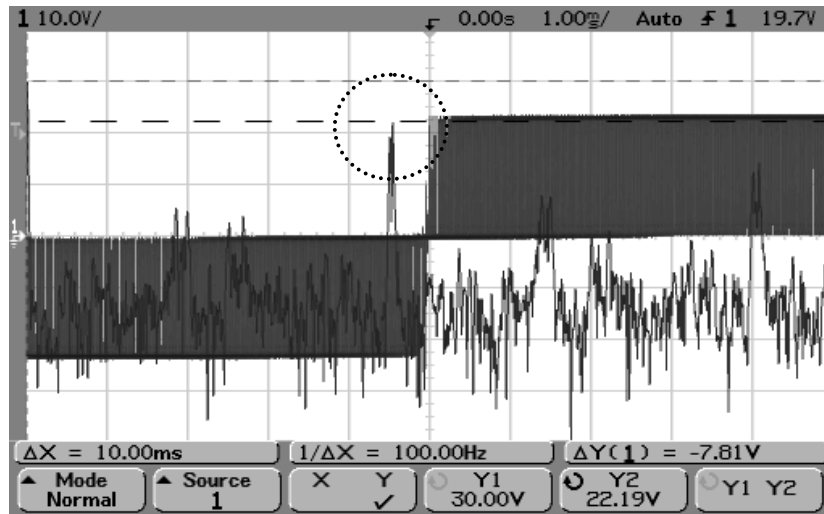
Figure 12. Determining the magnitude of the strongest high-frequency cluster with respect to the fundamental (the 46kHz cluster is 7.81V (in dB) down from the fundamental)

$$-7.81db = 20\log_{10}\left(\frac{V_{46kHz}}{V_{60Hz}}\right), \text{ so } \frac{V_{46kHz}}{V_{60Hz}} = 10^{\left(\frac{-7.81}{20}\right)} = 0.31.$$

Compare your calculations to the values in Table 1.

Similarly, for the $4f_{tri}$ cluster (i.e., approx. 92kHz), the values in Figure 21 yield

$$-16.6db = 20\log_{10}\left(\frac{V_{92kHz}}{V_{60Hz}}\right), \text{ so } \frac{V_{92kHz}}{V_{60Hz}} = 10^{\left(\frac{-16.6}{20}\right)} = 0.148.$$
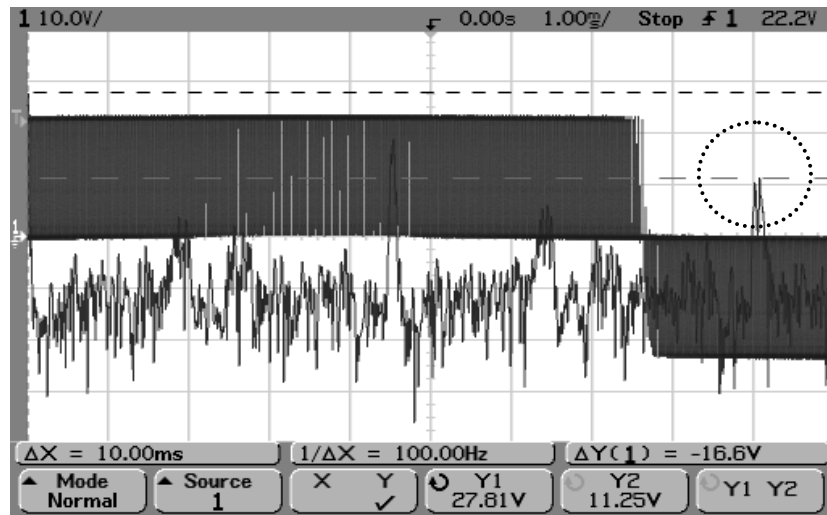
Compare your calculations to the values in Table 1.

Figure 13. Determining the magnitude of the second-strongest high-frequency cluster
with respect to the fundamental (the 92kHz cluster is 16.6db down from the
fundamental)

2. The lower-frequency harmonics of V_{cont} become much more significant in the
    overmodulation and saturation regions. With $0.90 < m_a < 1.0$, change the span to 1kHz, and
    the center frequency to 500Hz. Adjust the sample rate to 40kSa/s. The FFT results should be
    similar to those in Figure 14. Note that the harmonic multiples of 60Hz below 1kHz are at
    least 30db down from the fundamental (remember that 20db is a power of 10, 40db is a
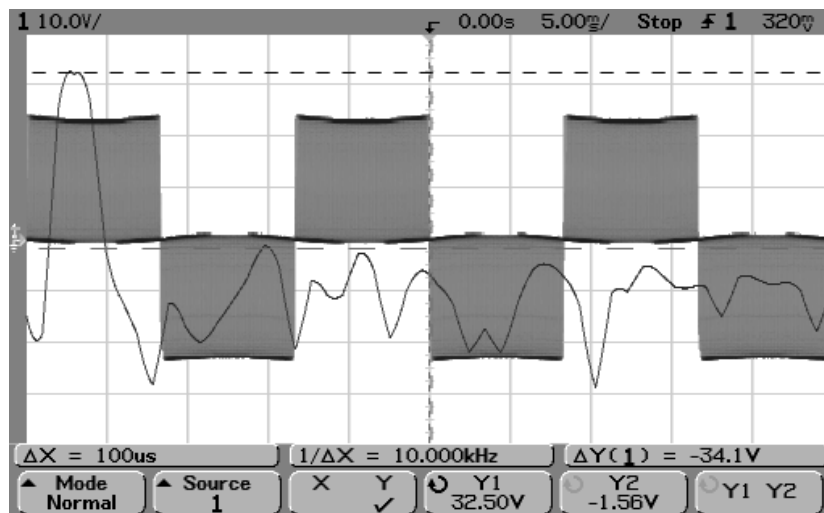   power of 100, and so on.

Figure 14. Low-frequency harmonics for $0.9 < m_a < 1.0$ are at least 30db down

3. Raise m_a to its maximum value so that you approach saturation. At this point, the waveform
    takes on the characteristics of a square wave, which has odd harmonics of the fundamental,

whose magnitudes decrease in proportion to harmonic order (i.e., the 3rd harmonic magnitude is 1/3 of the fundamental, and so on). Computations for Figures 15 and 16 show that the 3rd and 5th harmonic magnitudes are 0.30 and 0.13 of the fundamental, respectively.
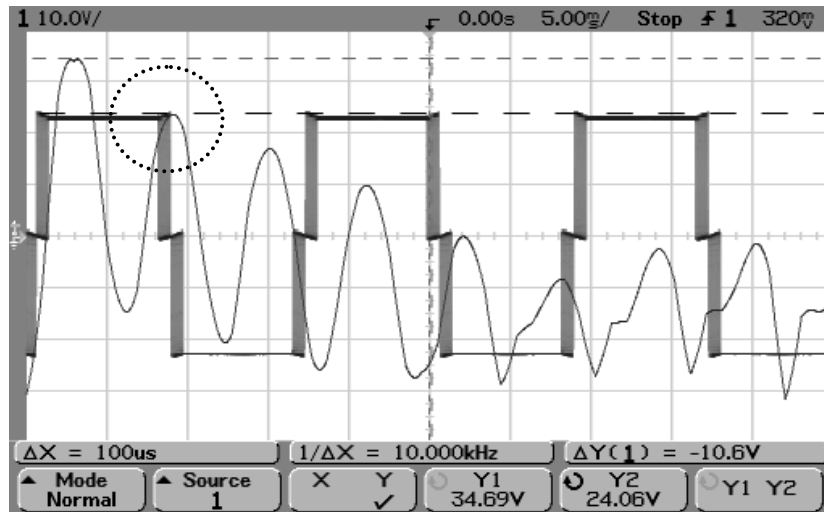

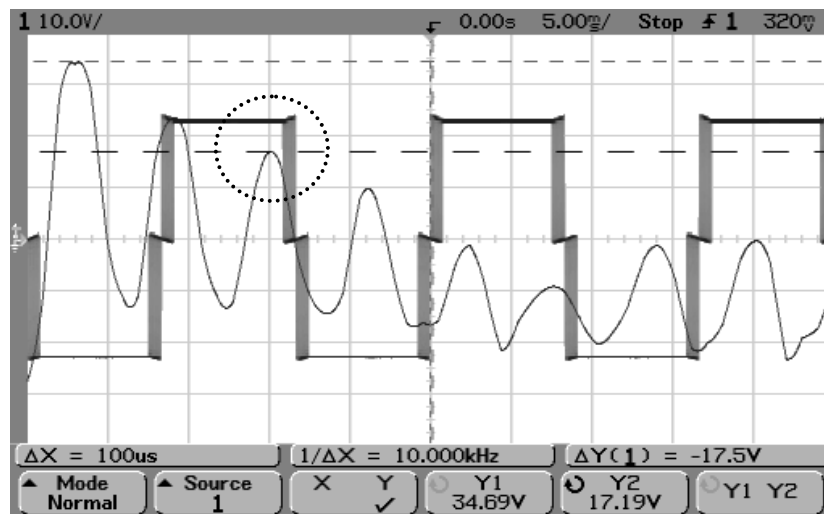Figure 15. Near saturation, the 3rd harmonic magnitude is 0.30 of the fundamental

Figure 16. Near saturation, the 5th harmonic magnitude is 0.13 of the fundamental

Reference
[1] N. Mohan, T. M. Undeland, W. P. Robbins, *Power Electronics – Converters, Applications, and Design*, 2nd Edition, John Wiley & Sons, Inc., 1995.

The ICs are powered by a 2W dual output DC-DC converter chip, 12Vdc input, isolated ±12Vdc outputs. Details for the dual output converter and its socket are shown below.
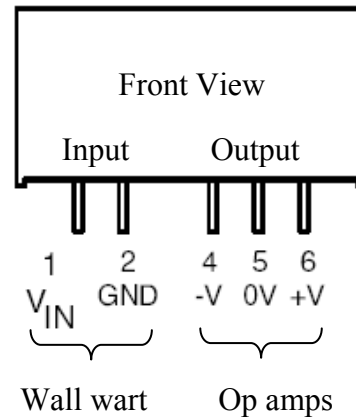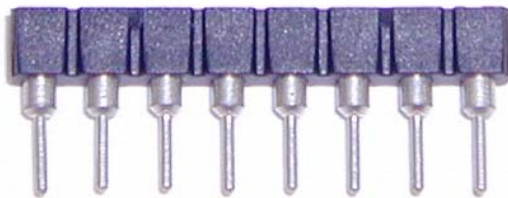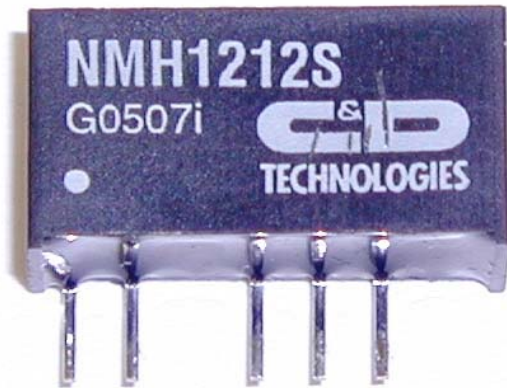
Notes for the above converter chip – **keep the input and output sections isolated from each other.**

When energizing your circuit, check the +12V and −12V outputs to make sure they are OK. Low voltages indicate a short circuit in your wiring, which can burn out the chip in a few minutes.

EE362L, Power Electronics, H-Bridge Inverter
Version Nov. 10, 2010

I. Introduction. In this experiment, you will build the H-Bridge portion of your inverter, connect your PWM control circuit to it, and then convert 35-40Vdc power to 60Hz ac, 100 – 200W.

II. Build the Circuit. DO NOT use fuses or fuse holders on the VDC side. **DO USE** a 10A fuse and holder on the VAC side. **DO NOT** use the optional output filter.

C1 = 0.1μF, 100V. C2 = 0.01μF, 100V.
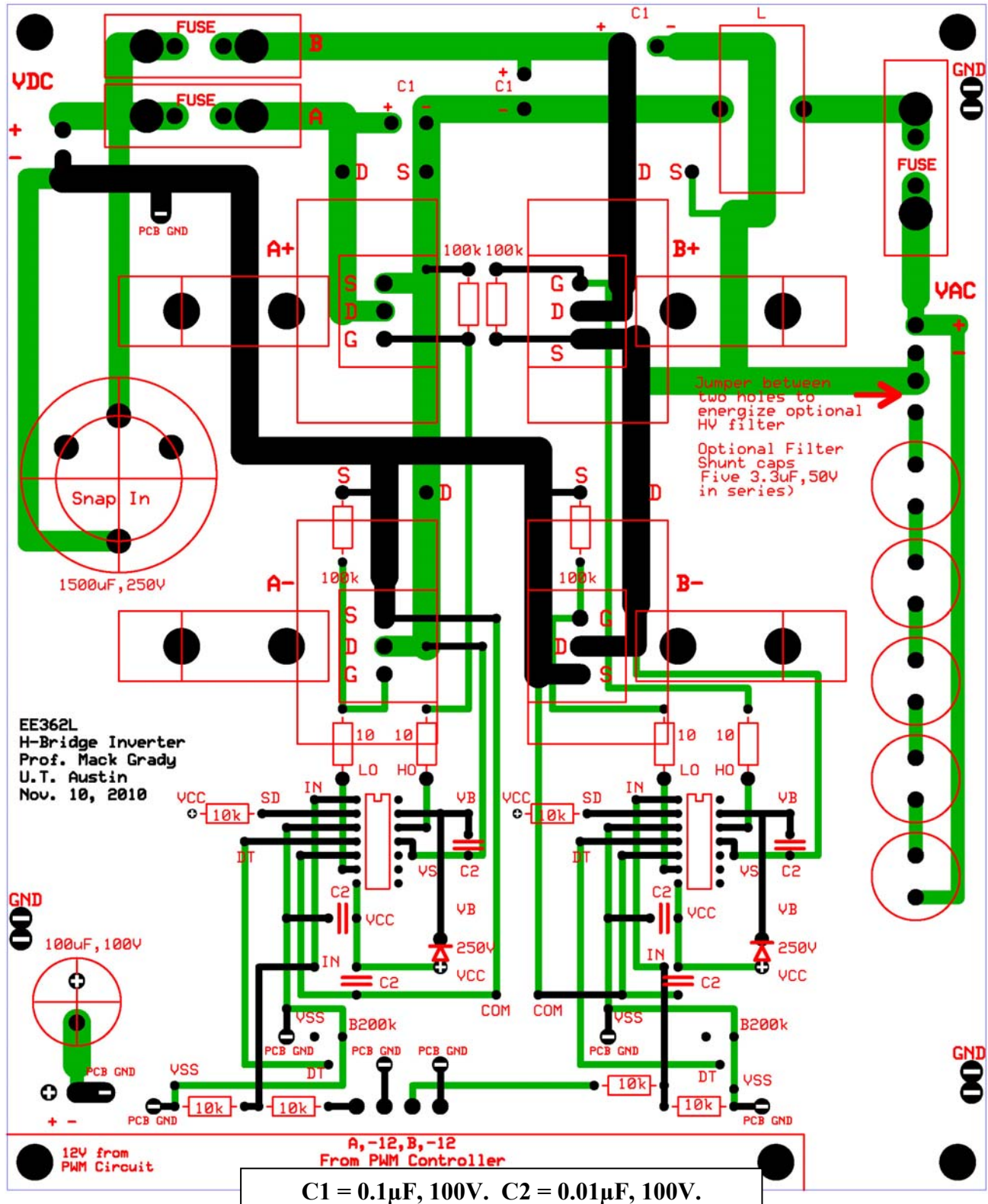
III. Initial Check of the A+/A- Side

Scope Probe 1 on Vdc

Both probe alligator clips on left side of L

Scope Probe 2 on Vdc reference

PC Board Reference (same as Vdc ref.)

Red text – see Step 11

1. Begin with DBR off and Variac at zero.
2. No wall-wart power to the H-Bridge.
3. No firing signals to the MOSFET gates
4. Solder a short #14 bare jumper wire "horseshoe" across the Vdc fuse holes that supplies A+ and A−.
5. While monitoring the ammeter, slowly raise Vdc to 40V. **Stop if more than 1A persists.** After the H-Bridge capacitor is quickly charged, the current should be negligible (less than 0.1A), else you have a bad connection somewhere.
6. Lower the variac to zero.

IV. Check of the A+/A− Side with m_a = 0.0

7. Connect your PWM Inverter Control Circuit to the H-Bridge.
8. Disconnect any Vcont input signals to your PWM Inverter Control Circuit so that m_a = 0.0.
9. Check triangle wave frequency and skewness. Adjust skewness if necessary.
10. Run wires from your DC wall wart jack to power the H-Bridge. One wall wart will power both PC boards. **Make sure that you power the H-Bridge directly from the wall wart, and not from the +12/−12 DC-DC chip output on the PWM Inverter Control Circuit.**
11. Connect scope probes as shown in the above figure, in preparation for simultaneously viewing MOSFET voltages $V_{DS}(A+)$, and $V_{SD}(A−)$. What we would really like to see is both $V_{DS}(A+)$ and $V_{DS}(A−)$, but to do that we would need a scope with isolated channels. For our purposes, $V_{SD}(A−)$ works fine.
12. Gradually raise Vdc to 40V **while making sure the DC current is negligible**.
13. Expect to see voltages as shown below in Figure 1.
14. Rotate the dead-time adjustment potentiometer and observe the impact on the waveforms. Is the dc current ever more than 0.1A?
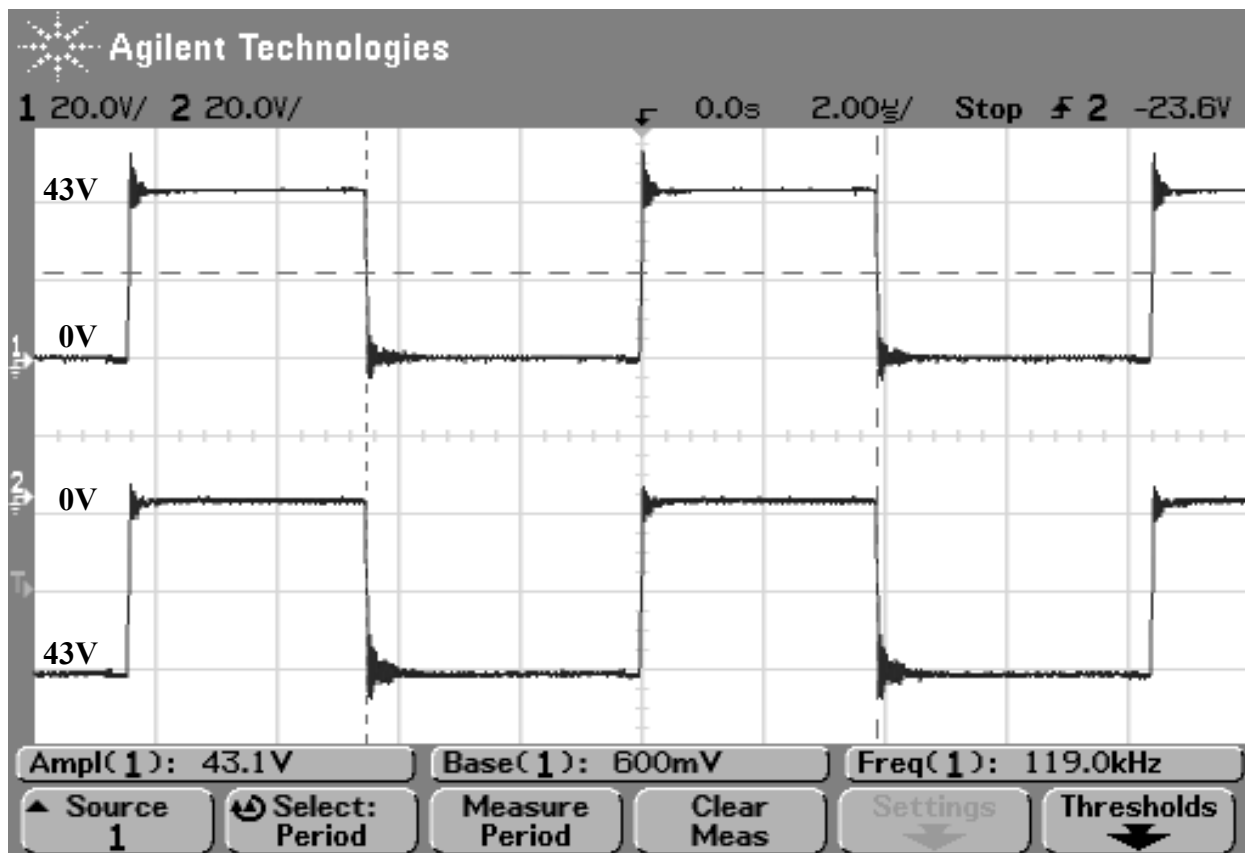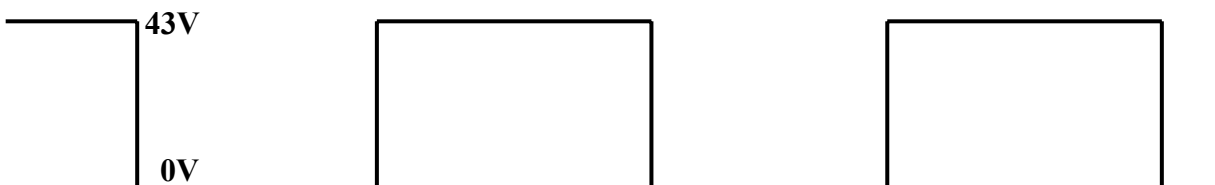15. Lower the variac to zero.

Figure 1. $V_{DS}(A+)$ and $V_{SD}(A-)$ with Vdc = 43V and $\mathbf{m_a = 0.0}$. The voltages should be **identical square waves, with 50% duty cycle, and static in appearance**.

If you view it, the corresponding VA with respect to VDC reference would have the following static appearance

V. Check of the A+/A− Side with $m_a \approx 1.0$

16. Apply a 60Hz, 4Vpeak sinewave from a benchtop waveform generator to your PWM Inverter Control Circuit. As in the previous lab, adjust the gain and −Vcont for a balanced (VA − VB) output that just below saturation so that ma ≈ 1.

17. Repeat the above steps for simultaneously viewing $V_{DS}(A+)$, and $V_{SD}(A-)$, checking for negligible DC current, and dead-time adjustment. A sample waveform is shown below in Figure 2.
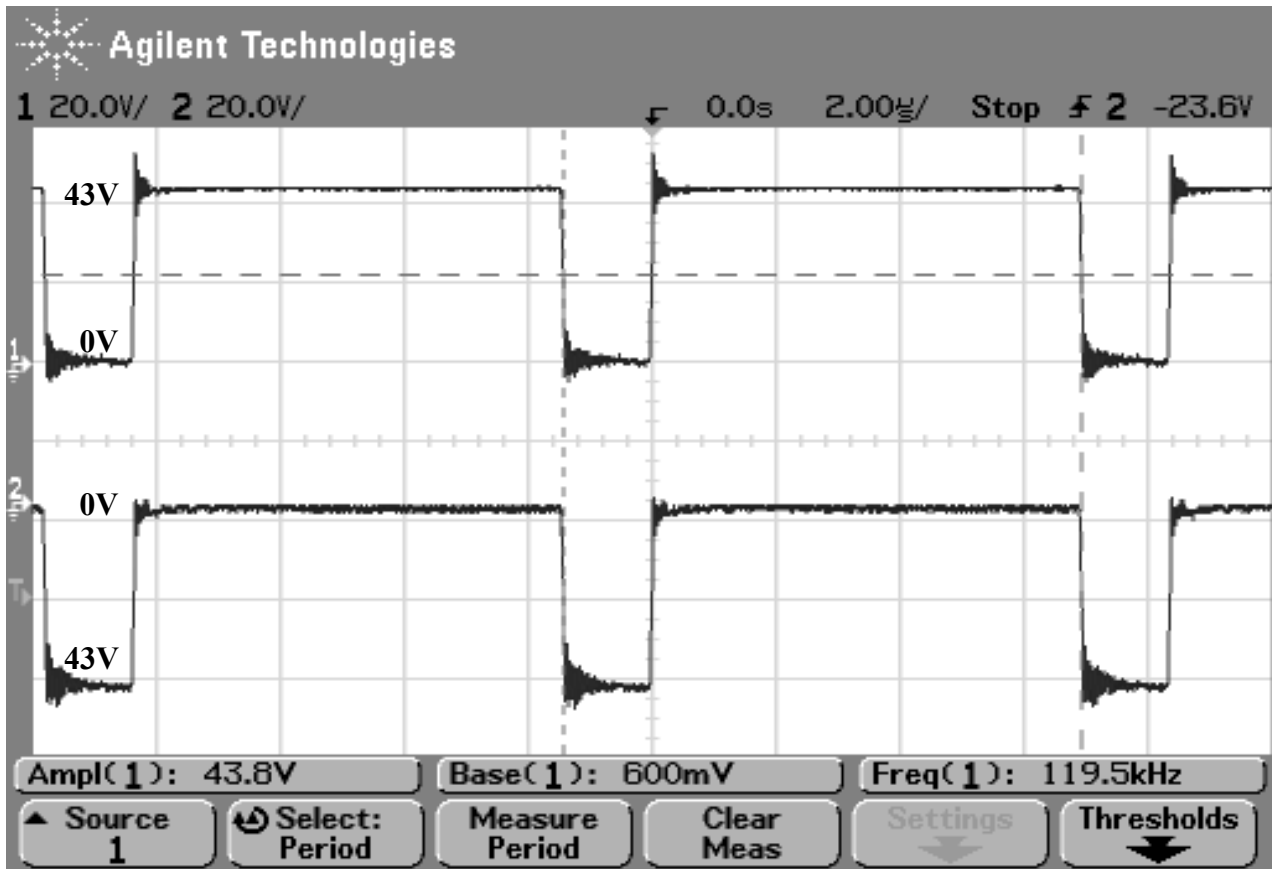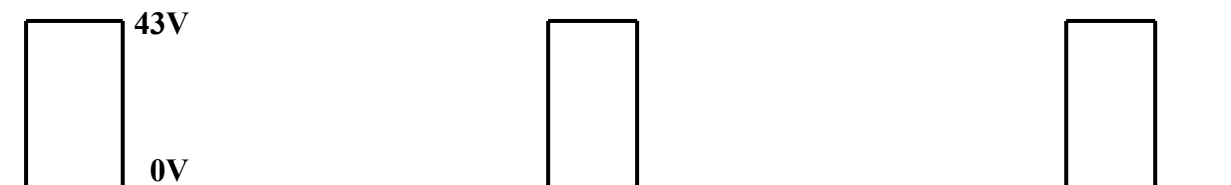
Figure 2. $V_{DS}(A+)$ and $V_{SD}(A-)$ with Vdc = 43V and **$m_a \approx 1.0$**. The voltages should be **identical rectangular waves, whose duty cycle varies with Vcont**..

If you view it, the corresponding VA with respect to VDC reference would have the following appearance, where the width of the pulses changes cyclically from smaller to wider and back to smaller for each cycle of 60Hz Vcont.

The modulation of pulse widths by sinusoidal Vcont produces the top half red-portion of the PWM wave construction chart presented in the previous lab.
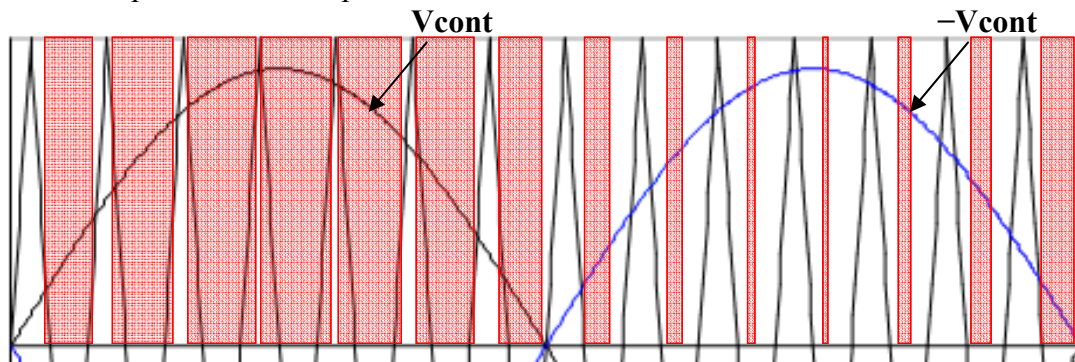
VI. Repeat the Above Steps for the B+/B− Side

- Leave the A+/A− side connected
- Solder a short #14 bare jumper wire "horseshoe" across the Vdc fuse holes that supplies B+ and B−.
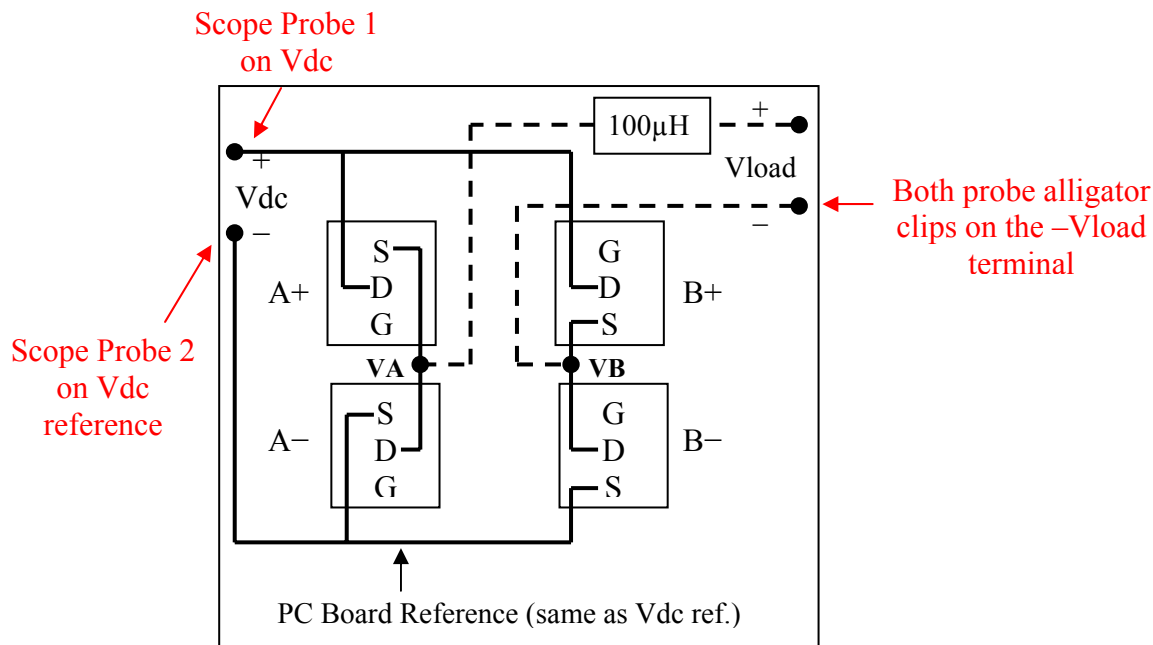- Move both probe alligator clips to the −Vload terminal

With the probe grounds moved to the −Vload terminal, the voltage waveforms should look the same as those you saw for the A+/A− side.

VII. Load Tests

You will now check your inverter performance with 100 to 200W of resistive load.
- Lower the variac to zero.
- Connect a 5Ω power resistor to the inverter output terminals Vload
- Connect a scope probe to observe Vload
- The benchtop waveform generator should be 60Hz sinusoidal, 4V peak.
- While viewing the ammeter, gradually increase the variac to the maximum clockwise rotation.

Here are my results. Compare yours to these.
- Triangle wave frequency = 120kHz, with a 2nF capacitor
- Adjust Vcont so that $m_a \approx 1$
- DBR output = 39.3Vdc, 2.5Adc, VI = 98W
- Vload(ac) = 20.5V, Vload(dc) = −0.02V, $V^2/R = 84W$
- After 5 minutes, the MOSFET heat sinks are **definitely warm**, but not too hot to keep your hand on them

- The voltage waveform appears sinusoidal except for some minor distortion at the zero crossings. The distortion may be due to 3rd harmonic.

Next, lower the variac to zero, add a second 5Ω power resistor in parallel so that the load is 2.5Ω, and repeat the test. My results are

- DBR output = 37.5Vdc, 4.5Adc, VI = 169W
- Vload(ac) = 18.5V, Vload(dc) is still negligible, V^2/R = 137W
- After 5 minutes, the MOSFET heat sinks are **hot to the touch**, too hot to keep your hand on them
- The voltage waveform is essentially unchanged

Next, lower the variac to zero, unplug the wall wart, and place a 0.01μF ceramic disk capacitor in parallel with your existing triangle wave chip capacitor. The new triangle wave frequency should be 15-20kHz. Repeat the 2.5Ω measurements. You will likely have to readjust Vcont to keep m$_a$ ≈ 1. My results are
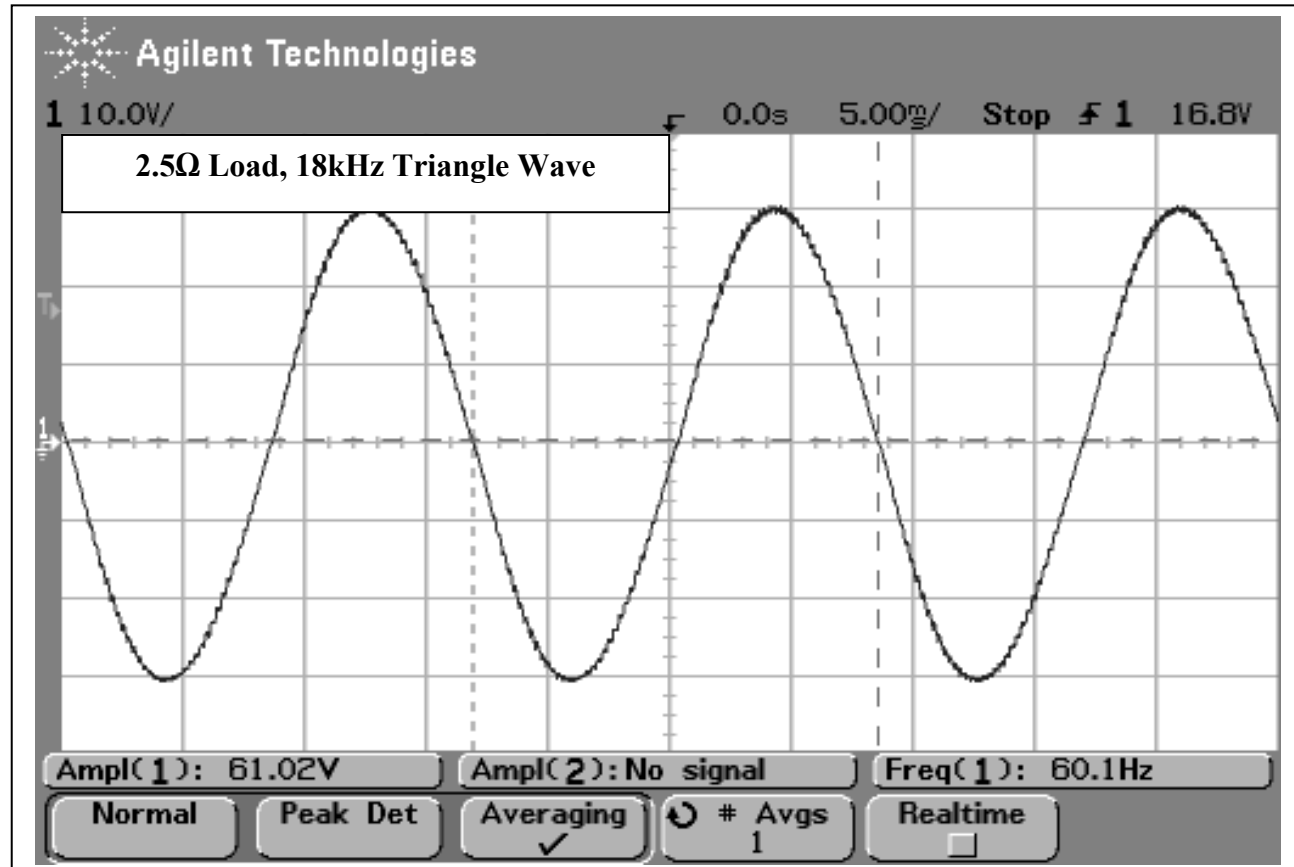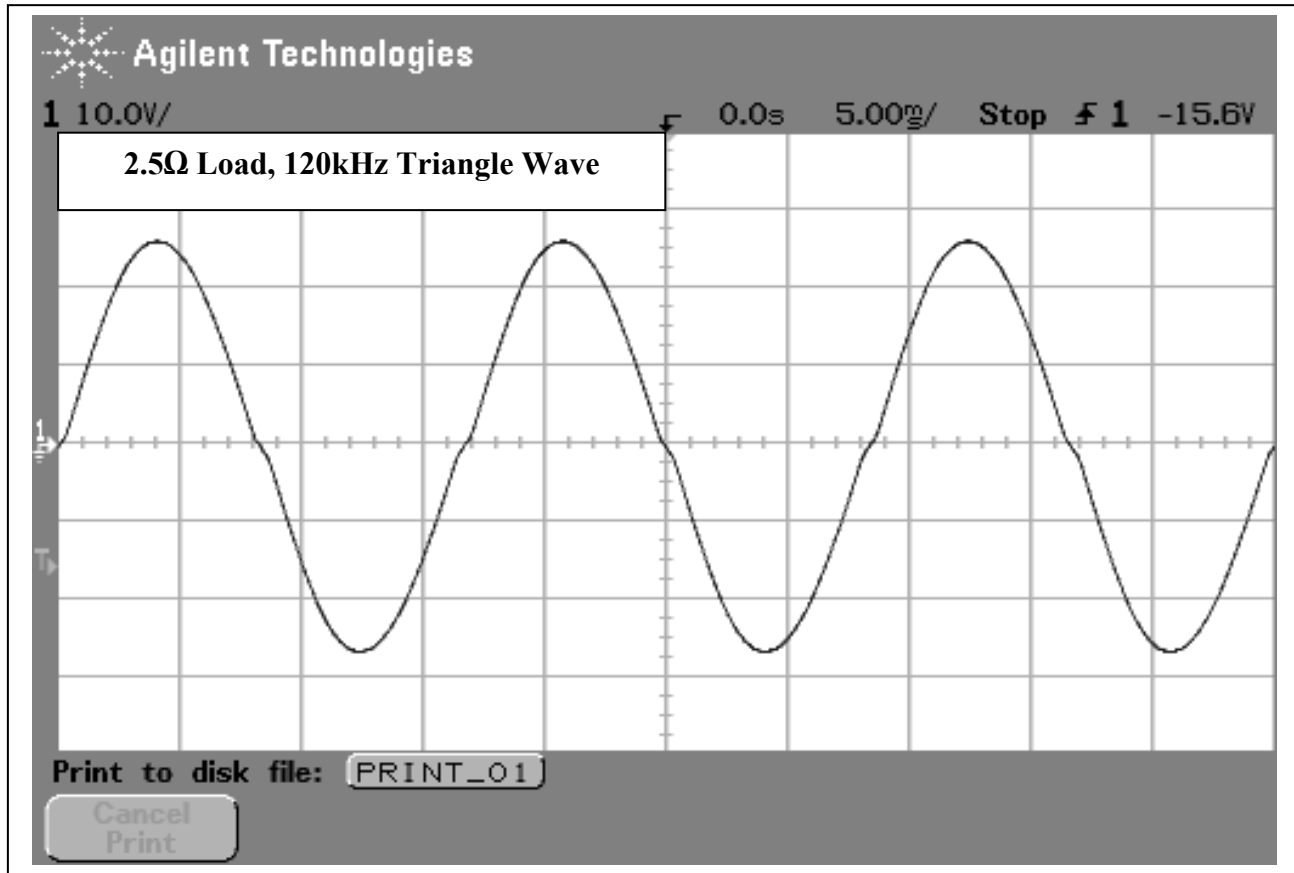
- DBR output = 35.3Vdc, 6.0Adc, VI = 212W
- Vload(ac) = 21.6Vrms, Vload(dc) still negligible, V^2/R = 187W
- After 5 minutes, the MOSFET heat sinks are **only slightly warm**
- The voltage waveform appears sinusoidal

Corresponding screen snapshots are shown below.

2.5Ω Load, 120kHz Triangle Wave

2.5Ω Load, 18kHz Triangle Wave

International
IR Rectifier
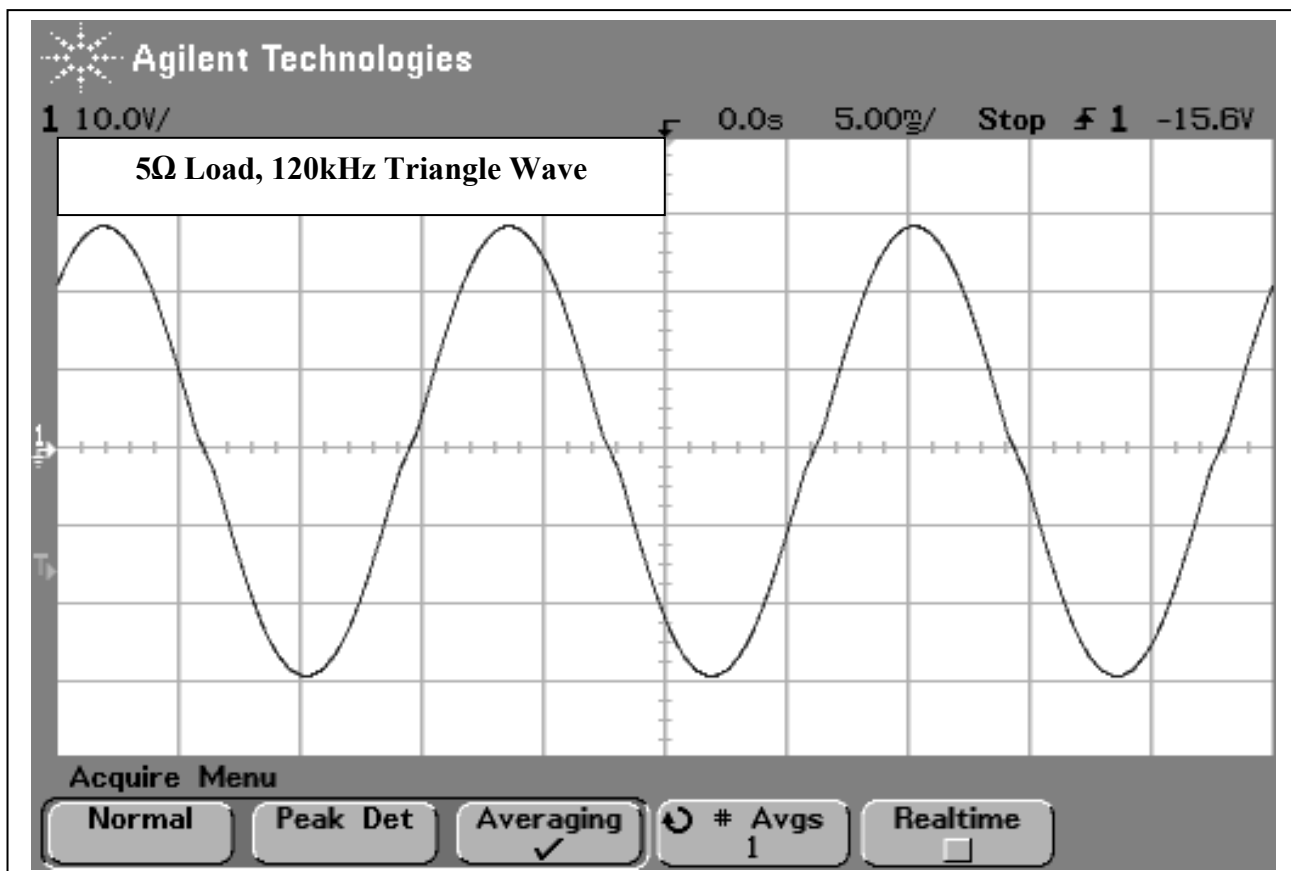
IRS2184/IRS21844(S)PbF
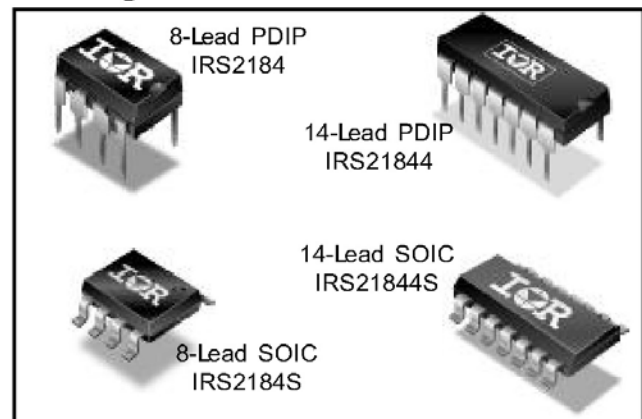
HALF-BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V and 5 V input logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5 V offset
- Lower di/dt gate driver for better noise immunity
- Output source/sink current capability 1.4 A/1.8 A
- RoHS compliant

Packages

8-Lead PDIP
IRS2184

14-Lead PDIP
IRS21844

14-Lead SOIC
IRS21844S

8-Lead SOIC
IRS2184S

Description

The IRS2184/IRS21844 are high volt-age, high speed power MOSFET and IGBT drivers with dependent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic in-put is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse cur-

Feature Comparison

Part	Input logic	Cross-conduction prevention logic	Deadtime (ns)	Ground Pins	t_{on}/t_{off} (ns)
2181	HIN/LIN	no	none	COM	180/220
21814				Vss/COM	
2183	$\overline{HIN}$/LIN	yes	Internal 400	COM	180/220
21834			Program 400-5000	Vss/COM	
2184	IN/$\overline{SD}$	yes	Internal 400	COM	680/270
21844			Program 400-5000	Vss/COM	

rent buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

Typical Connection

IRS2184
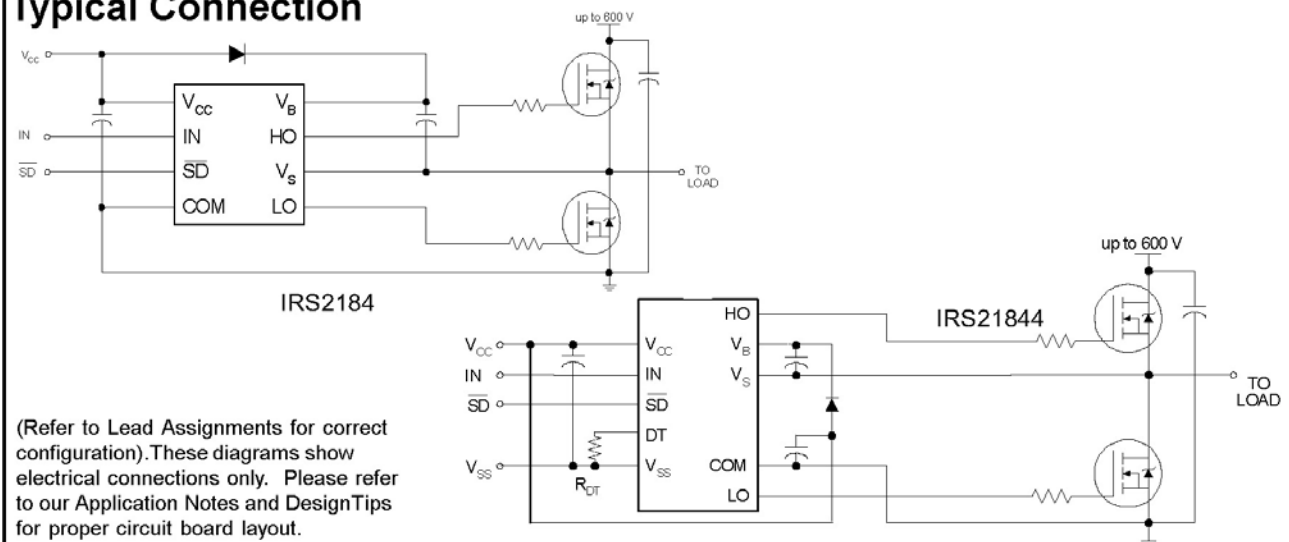
(Refer to Lead Assignments for correct configuration).These diagrams show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

IRS21844

H_Bridges_Fixes. Nov. 16, 2010. Here are the changes described on Monday. If you have already completed the H-Bridge lab measurements successfully, no need to re-run. But make the changes now in preparation for upcoming labs, and re-test your circuit with a 5 Ω load.

EE462L
PWM Control Circuit
Prof. Mack Grady
Oct. 28, 2010

Use 1.5 nF. Yields about 130kHz triangle wave

X means to remove component
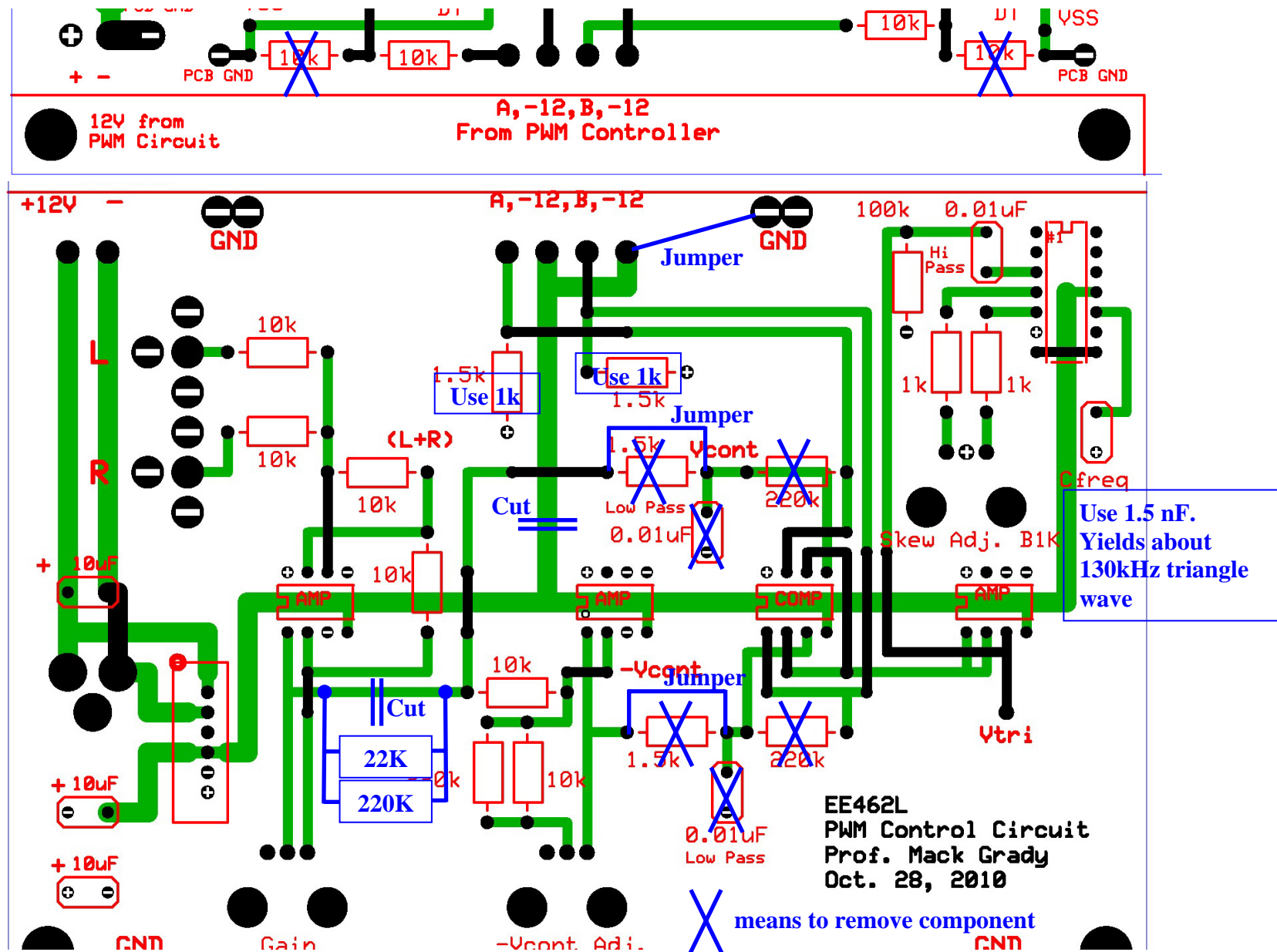
Introduction
This lab is "credit" or "no credit." There is no formal lab report. You will demonstrate the use of your inverter as an audio amplifier in person to a TA or Dr. Grady, using our laptop PC as a waveform generator and music source, and a 32Ω speaker unit.

"Credit" requires that
* All inverter modifications have been made,
* Your inverter produces a near-perfect sinewave output,
* Your inverter's sound quality meets or exceeds our expectation,
* Both partners are present,
* You complete your demonstration before Thanksgiving.

Your demonstration can be during your lab session or according to a sign-up sheet of 15-minute time slots. **A 15-minute slot is adequate only if your inverter is working properly before you begin.**

Due to tight scheduling, you cannot run over your time slot if another customer is waiting. If you cannot finish in 15-minutes, sign up for another time slot.

It is OK for you to practice ahead of time if the music station is not busy. It is also OK to enjoy playing music using your own iPod or laptop, provided you do not disturb others.

The laptop should remain "on," but just in case, the password is oglesby. The directory you need is EE462L, which has a shortcut near the top right of the screen. The PC's volume settings (lower right icon) should be at the max.

Setup
Connect the 0-15Vdc power supply to your inverter, and your inverter to the speaker unit. The speaker unit has four 8Ω speakers in series, so the inverter load will be 32Ω resistive. The maximum average power going to the speaker unit for $m_a \leq 1.0$ linear operation will be

$$P_{spea\ker} = \frac{\left(V_{dc}/\sqrt{2}\right)^2}{R_{spea\ker}} = \frac{15^2/2}{32} = 3.5\,Watts$$. However, when you observe the voltmeter and

ammeter on the 0-15Vdc power supply, you will see that the current is typically very small (less than 0.1 A). This means that the average power drawn from the Vdc power supply probably never exceeds 2 Watts. Music "punch power" is provided in bursts by your inverter's 1500µF high-frequency capacitor. For more "punch," simply add more µF.

To block any DC current that your inverter might produce, the 32Ω speaker unit is connected in series with 15-paralleled 33µF high-frequency ac capacitors, totaling 495µF. The RC time constant for 32Ω and 495µF is 16msec, which corresponds to a low freq cut-off of 10Hz. A 1µF high-frequency capacitor is added across the input terminals to improve scope viewing.

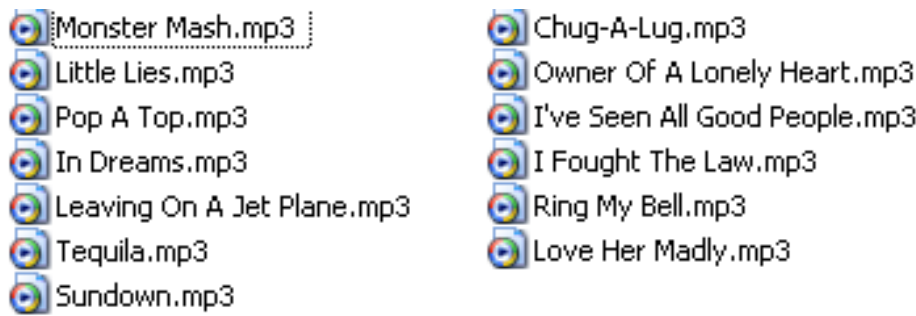**The Middle-C Sinewave Test (Observed by a TA or Dr. Grady)**
Middle-C is a 261.626 Hz sinewave. To produce it,
* Attach the two audio jacks from the PC to your PWM controller.

- Connect a scope probe to view V(L + R) on your PWM controller.
- In PC directory EE462L, double-click on "Harmonic_V_I_Waveform_Generator_100315.xls," which is an Excel-Visual Basic program.
- Click on the orange "Start" button.
- When the user interface screen appears, click on "Start Program."
- Click on the "Middle C (Octave 4)" button The PC will play out Middle C with a peak voltage of about 3V. View V(L + R) on the scope – it should be a perfect sinewave.
- Move the scope probe to your inverter's output. Use the scope's filter function.
- Attach the Vdc power supply to your inverter and raise Vdc to about 5V.
- Raise your PWM controller gain until you reach overmodulation, then back off just into the linear region. Note the speaker buzzing as you went into overmodulation.
- From now on, do not touch the PWM controller gain. The power supply Vdc will be your volume control.
- Raise Vdc to 15V. The speaker voltage waveform on the scope should be a near perfect sinewave with about 10V peak. A 10V peak sinewave applied to 32Ω produces about 1.5 Watts.
- The proper way to exit the program is to click on "Stop Program."
- Lower Vdc to zero.

The Music Test (observed by a TA or Dr. Grady)
You will now use the PC to play MP3 files. The choices in the directory are:

Monster Mash.mp3	Chug-A-Lug.mp3
Little Lies.mp3	Owner Of A Lonely Heart.mp3
Pop A Top.mp3	I've Seen All Good People.mp3
In Dreams.mp3	I Fought The Law.mp3
Leaving On A Jet Plane.mp3	Ring My Bell.mp3
Tequila.mp3	Love Her Madly.mp3
Sundown.mp3	

- Connect a scope probe to view V(L + R) on your PWM controller.
- Click on one of the MP3 files to play it with Windows Media Player.
- Raise and lower Media Player's volume control and observe clipping on the scope. Clipping occurs at about 3V. Lower Media Player's volume control until there is no evidence of clipping. We suggest 33 as the setting.
- Move the scope probe to your inverter's output. Use the scope's filter function.
- The power supply Vdc is now your volume control.
- Play the music, paying attention to the waveform and sound quality.

Get Your Grade
A TA or Dr. Grady will sign-off on our sheet, Credit or No-Credit. If No-Credit, sign up for another slot.

1. Overview

You will your PI controller with a buck converter to efficiently step down a solar panel pair voltage to a regulated 13.8V for safely powering automotive-type equipment. Because the MOSFET source terminal of a buck converter is not the same as the converter's reference, some form of isolation between the Vout of the converter and the PI controller feedback terminal is needed. This can be in the form of an isolated MOFET driver chip, or some other more general form of optical isolation. In this experiment you will use an International Rectifier Photovoltaic Isolator, PVI1050N. The PV chip has two halves, each with an internal LED light source and tiny solar cells whose short circuit current is proportional to the LED current. We series the input LEDs, and parallel the output cells.

2. The Circuit

Buck converter Vout

This is the αVout to your PI controller. Remove the PI voltage divider circuit and feed this signal in directly as αVout.
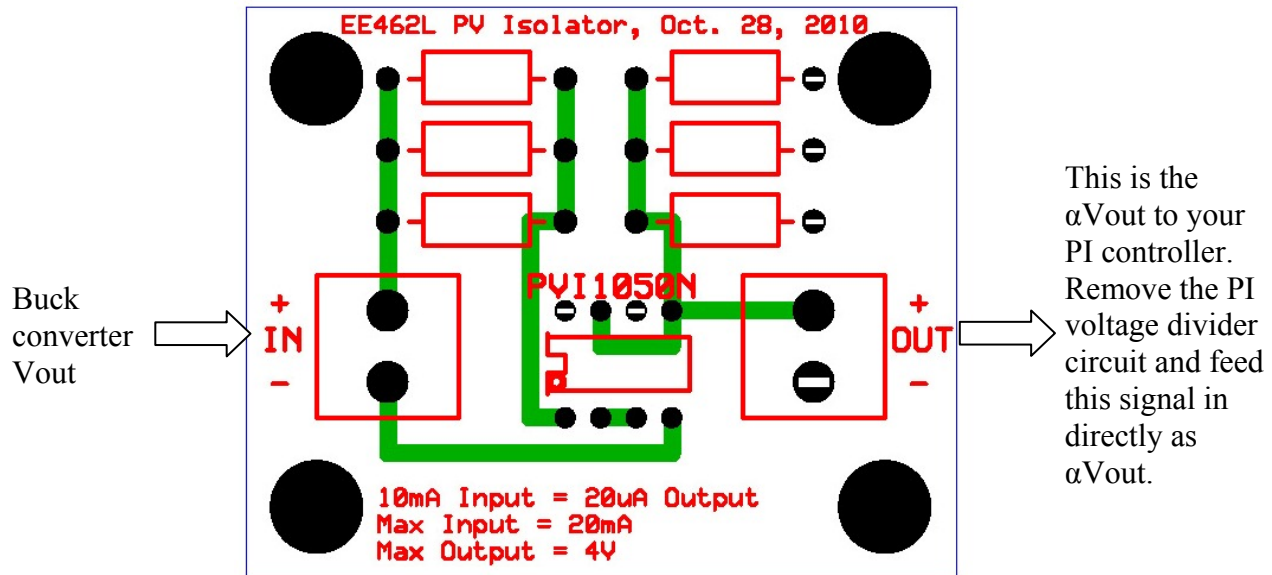
Figure 1. PV Isolator Circuit

The circuit needs two biasing resistors – one for input, and the other for output. Extra slots are provided in case you use parallel combinations.

3. Select the Resistor Values

Select the input resistor so that max buck converter output voltage (40V from the panels) produces rated PV chip current (20mA). 40V rated will provide plenty of headroom to see overshoots on the normal 13.8V output of the buck converter. Example: 40V / 20mA = 2000Ω. Use 2.2kΩ. Resistor power check, $40^2/2200 = 0.73W$. Thus, use two 4.7kΩ, ½ W resistors in parallel.

20mA PV chip input current produces 40µA PV chip output short circuit current. In this case, "short circuit" means that the output voltage is less than PV chip rated 4V output. 40µA through a 100kΩ resistor yields 4V. Power check = tiny. Thus, use 100kΩ.

4. Apply 13.8Vdc to the PV Isolator Circuit and Measure αVout (which will be your PI Set Point Voltage)

5. Optional Linearity Checks with Oscilloscope

Figure 2. 100Hz Vin. DC offset added toVin so that Vin is sinusoidal between 5V and 12.1V. Corresponding Vout is in phase and appears linear with 0.938Vpeak

Freq(1): 100.8Hz   Max(1): 12.10V   Max(2): 938mV

Figure 3. Same as Figure 2, but at 1kHz. Identical to Figure 2, proving that the PV chip is responding well to 1msec signals.

Freq(1): 1.005kHz   Max(1): 12.00V   Max(2): 922mV

Figure 4. Same as Figure 2, but at 10kHz. Output is reduced compared and has noticeable phase delay

Figure 5. 100Hz Vin, with DC Offset Removed. Vin raised to 10V peak. Clearly shows the forward bias dead band and inability to track negative inputs.

EE462L, Power Electronics, Powering the Grid with Renewable Energy
Version November 22, 2010

Introduction
You have successfully built a DC-AC inverter. You will now use your inverter to convert DC to AC and send power back into the AC grid. Your grid access point is a 120V wall outlet. **Make sure that your inverter is working properly before beginning this experiment.**

To begin with, you will use a 100Vdc bus created by a variac + isolation transformer + special DBR that is rated for that voltage. **So be careful!** Later, if there is good sun, you can one of our 40V (open circuit) solar panel pairs and feed its DC power into to the grid.

## Steady-State AC Equivalent Circuit of the H-bridge Inverter
Consider the H-bridge inverter circuit illustrated below. We have observed in the H-bridge experiment that when V_{cont} is steady-state AC, and MOSFET firing is controlled using unipolar PWM, and inverter output is properly filtered, then the equivalent circuit "seen" by the load (e.g., motor) has a dominant sinusoidal component.
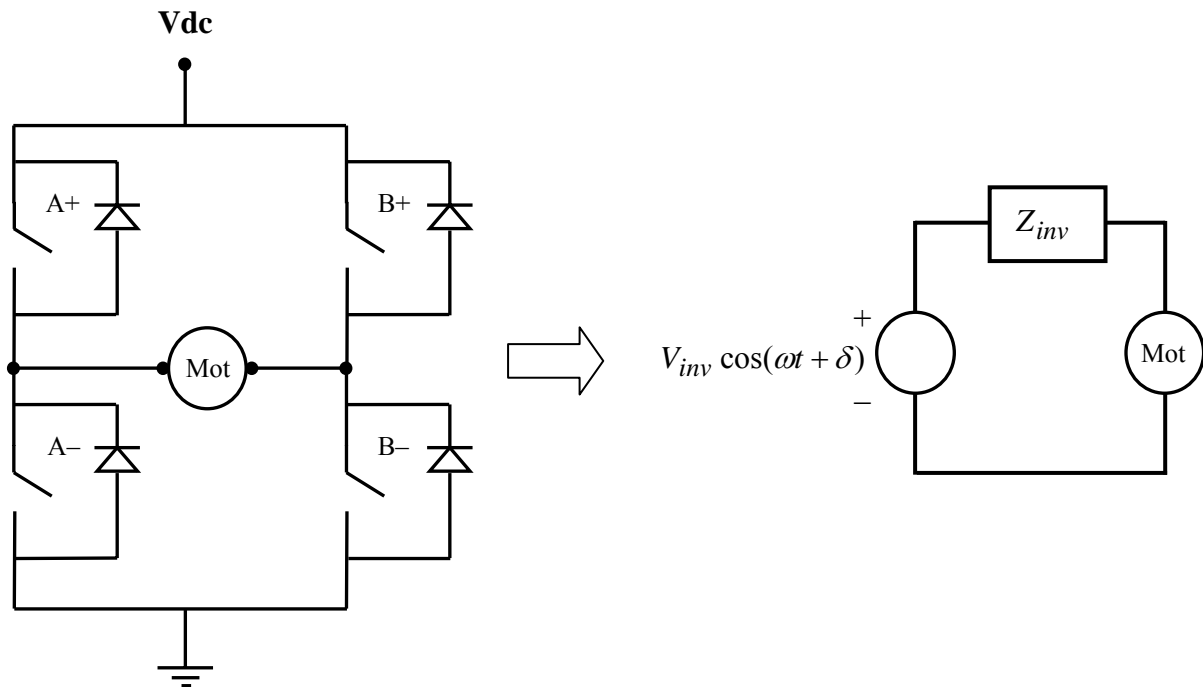
In the above figure, $V_{inv} = \dfrac{V_{dc}}{\sqrt{2}} \bullet m_a$ rms volts, and Z_{inv} is the impedance of the inverter at the AC operating frequency. Unless a very large inductor is intentionally added to the inverter output, Z_{inv} is mostly resistive in low voltage (i.e., less than 1kV) circuits.

Re-examination of the H-Bridge Circuit
The H-bridge is not limited to inverter operation. For example, without changing circuit topology, move the motor to the left, outside the bridge, as shown on the next page.
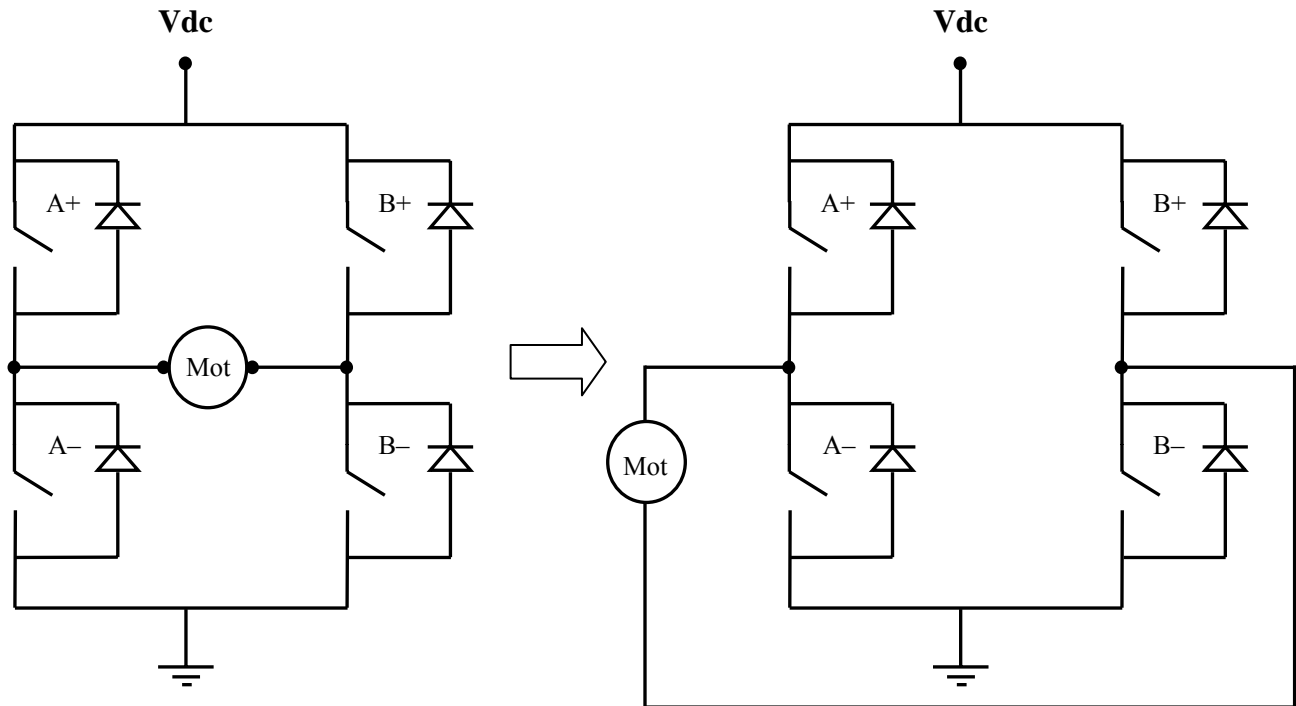
Now, move the DC terminals to the right, and replace Vdc with a capacitor. Then, replace the motor with an AC source.
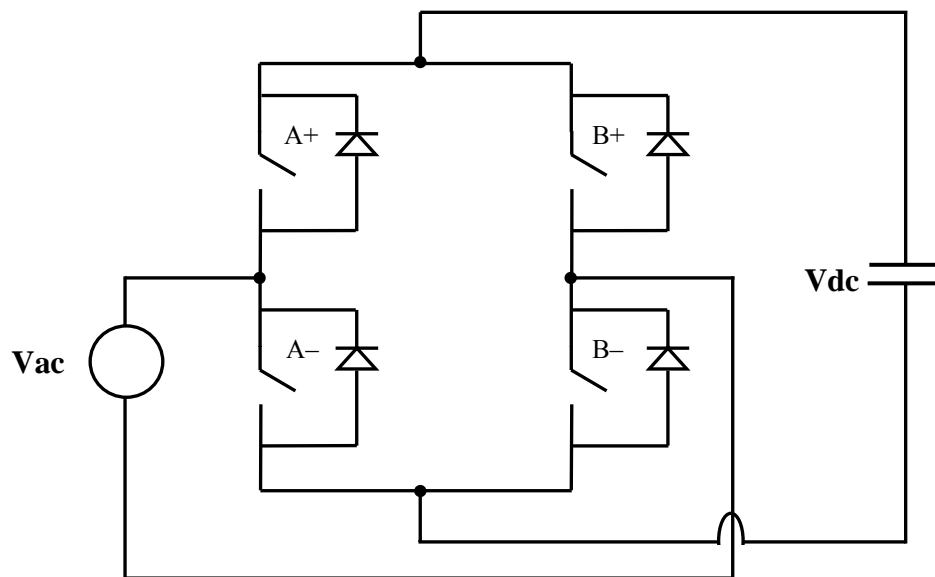
You can see that if the MOSFETs are never switched "on," the above circuit behaves like a DBR circuit because of the internal diodes of the MOSFETs! Thus, it is clear that the H-bridge circuit can also be a rectifier (like the DBR), where power moves from the AC side to the DC side. Thus, by controlling the firing of the MOSFETs, the H-bridge can be either a rectifier or an inverter.

Control of Power Flow into the Grid
Consider the AC equivalent, but replace the motor with the grid (i.e., a wall outlet, either hard-wired or scaled down using a variac). The grid has some impedance, but it is much smaller than the inverter impedance.
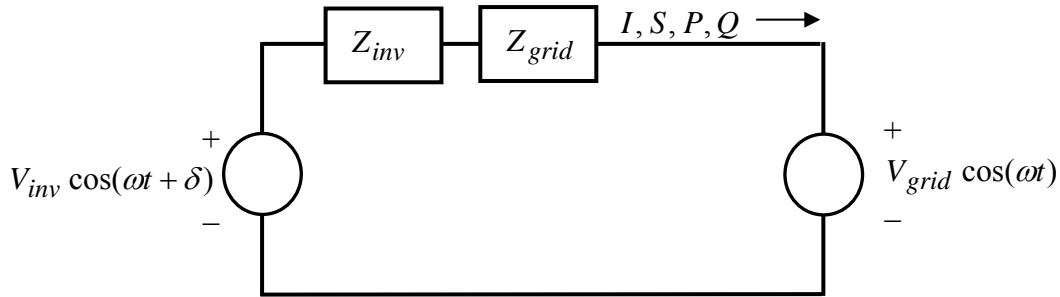
The phasor current that flows is

$$I = \frac{V_{inv} \angle \delta - V_{grid} \angle 0}{Z_{inv} + Z_{grid}} \ ,$$

and the complex power, active power, and reactive power flowing into the grid are

$$S = V_{grid} I^*, \ P = real(S), \ Q = imaginary(S).$$

Define

$$Z_{tot} = Z_{inv} + Z_{grid} \ , \text{ where } Z_{tot} = R_{tot} + jX_{tot} \ .$$

Then

$$S = V_{grid} \angle 0 \bullet \left(\frac{V_{inv} \angle \delta - V_{grid} \angle 0}{Z_{tot}} \right)^* = \frac{\left(V_{grid} V_{inv} \angle - \delta\right) - \left(V_{grid}^2\right)}{R_{tot} - jX_{tot}} \ .$$

Expanding yields

$$S = \frac{V_{grid} V_{inv}\left(\cos(-\delta) + j\sin(-\delta)\right) - V_{grid}^2}{R_{tot} - jX_{tot}} = \frac{V_{grid} V_{inv}\left(\cos\delta - j\sin\delta\right) - V_{grid}^2}{R_{tot} - jX_{tot}} \ . \tag{1}$$

The Resistive Impedance Case (typical for circuits below 1kV)

Now, consider the usual low-voltage situation where $R_{tot} \gg X_{tot}$. Then

$$S = \frac{V_{grid}V_{inv}\left(\cos\delta - j\sin\delta\right) - V_{grid}^2}{R_{tot}} = \frac{V_{grid}V_{inv}\cos\delta - V_{grid}^2 - jV_{grid}V_{inv}\sin\delta}{R_{tot}}$$

$$= \frac{V_{grid}}{R_{tot}}\left(V_{inv}\cos\delta - V_{grid}\right) - j\frac{V_{grid}V_{inv}}{R_{tot}}\sin\delta \;.$$

Thus, when X_{tot} is neglected,

Resistive impedance case: $\quad P = \dfrac{V_{grid}}{R_{tot}}\left(V_{inv}\cos\delta - V_{grid}\right),$ $\qquad\qquad$ (2)

Resistive impedance case: $\quad Q = -j\dfrac{V_{grid}V_{inv}}{R_{tot}}\sin\delta \;.$ $\qquad\qquad$ (3)

Thus, when X_{tot} is neglected, then P is proportional to $\left(V_{inv}\cos\delta - V_{grid}\right)$. Clearly V_{inv} must be greater than V_{grid} for inverter action to occur. In our lab experiment, angle δ is zero because the inverter control signal is a replica of V_{grid}. **Thus, for the resistive case in our experiment, ($V_{inv} - V_{grid}$) controls P, and Q is zero.**

The Inductive Impedance Case (typical for circuits higher than several kV)

Now, consider the alternate case, i.e., $X_{tot} \gg R_{tot}$, as might occur if a large series inductor is inserted in the power path. Re-evaluating (1) yields

$$S = \frac{V_{grid}V_{inv}}{X_{tot}}\sin\delta + j\frac{V_{grid}}{X_{tot}}\left(V_{inv}\cos\delta - V_{grid}\right).$$

Thus, when R_{tot} is neglected,

Inductive impedance case: $\quad P = \dfrac{V_{grid}V_{inv}}{X_{tot}}\sin\delta,$ $\qquad\qquad$ (4)
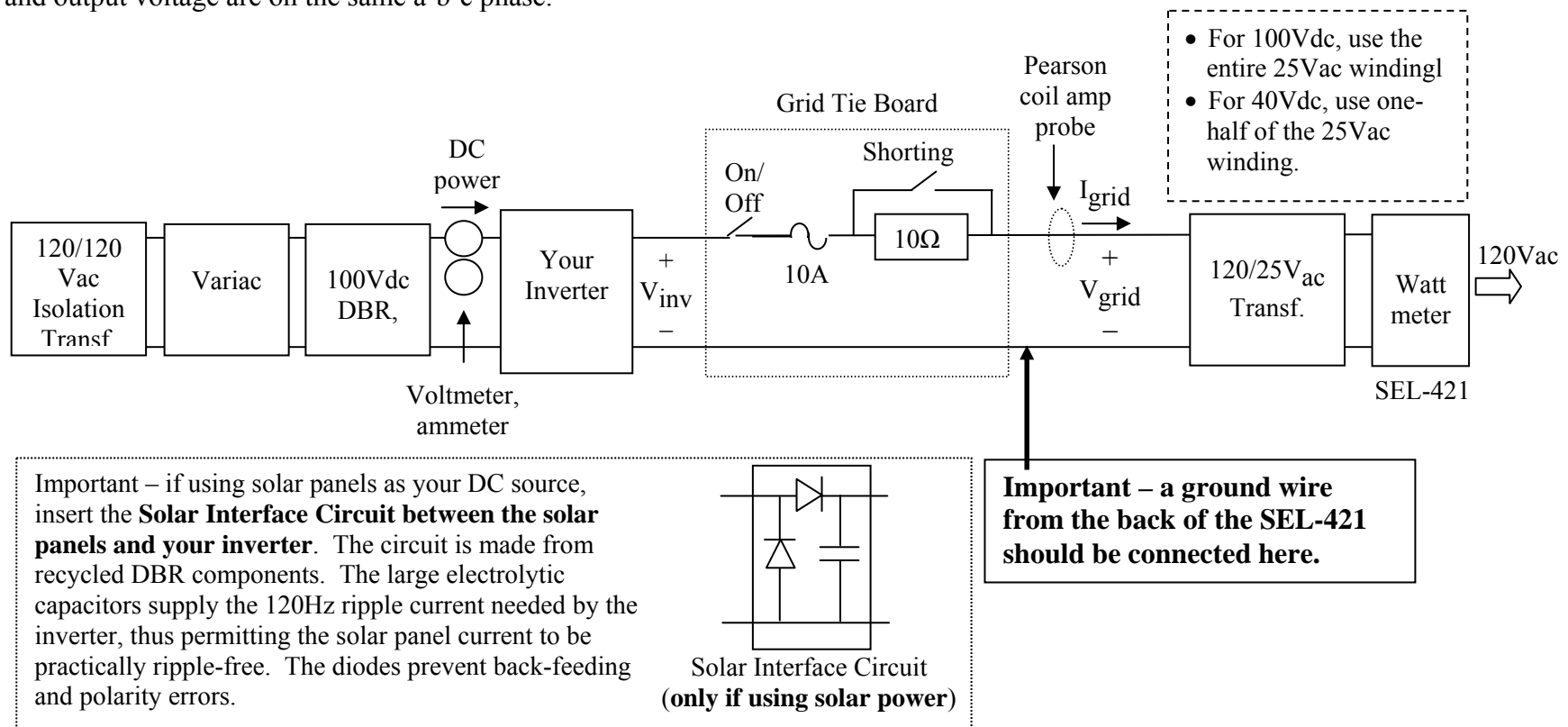
Inductive impedance case: $\quad Q = \dfrac{V_{grid}}{X_{tot}}\left(V_{inv}\cos\delta - V_{grid}\right).$ $\qquad\qquad$ (5)

Thus, for the inductive case, angle δ controls P, and V_{inv} controls Q.

The Experiment
Make sure that your inverter is working properly before beginning this experiment. Be considerate of others who are waiting.

To send power back to the grid, it is essential that V_{cont} be a scaled-down version of the AC grid voltage so that there is no phase shift or frequency error introduced. In a commercial building, such as ENS, wall outlets are distributed among the three phases (i.e., a-b-c) to balance the load. The three phases have 120° phase spacing. **To avoid a 120° error in phase shift, it is important that you plug your AC wall wart into the same lab bench to which you will send power**. That way, you can be assured that your control voltage and output voltage are on the same a-b-c phase.

- For 100Vdc, use the entire 25Vac windingl
- For 40Vdc, use one-half of the 25Vac winding.

Pearson coil amp probe

Grid Tie Board

DC power

Shorting

On/Off

I_{grid}

10Ω

10A

120/120 Vac Isolation Transf

Variac

100Vdc DBR,

Your Inverter

$+ V_{inv} -$

$+ V_{grid} -$

120/25Vac Transf.

Watt meter

120Vac

SEL-421

Voltmeter, ammeter

Important – if using solar panels as your DC source, insert the **Solar Interface Circuit between the solar panels and your inverter**. The circuit is made from recycled DBR components. The large electrolytic capacitors supply the 120Hz ripple current needed by the inverter, thus permitting the solar panel current to be practically ripple-free. The diodes prevent back-feeding and polarity errors.

Solar Interface Circuit
(**only if using solar power**)

Important – a ground wire from the back of the SEL-421 should be connected here.

1. Make sure the two knife switches on the Grid Tie Board are open.
2. Make sure that the variac is off and turned all the way down.
3. Make sure that the ground wire from the SEL-421 is connected to the point shown in the previous figure.
4. Connect a 12Vdc wall wart to your inverter jack, and the yellow-painted AC wall wart (with audio plug) to Vcont.
5. Connect the input DBR to your inverter, and slowly bring up the variac so that Vdc is about 40V. Idc should remain zero for now.
6. View Vinv and Vgrid on a scope. **They should be in phase**. If 180 degrees out of phase, reverse the yellow-painted AC wall wart.
7. Adjust ma until about 1.0.
8. Check the rms voltage of Vinv and Vgrid with a multimeter. Adjust Vdc until Vinv is within 2 volts of Vgrid.
9. The two voltage waveforms should now have approximately the same magnitude on the scope.
10. The Shorting knife-switch stays OPEN for now. Close the On/Off knife-switch on the Grid Tie Board, which connects the inverter to the grid through the 10ohm power resistor.
11. If no sparks, buzzing, or Idc, close the shorting knife-switch. Bring up the variac so that about 3A of dc current flows. This should occur at about 70Vdc, which means that your inverter is receiving about 200W of DC power
12. View the power flow on the SEL421. The reading will be negative, which means that power is flowing back into the wall outlet. If the SEL is not properly set up to read power, then do the following::
    A. Press ENT to reach the "Main Menu," then
    B. Press ENT to reach the "Meter Menu," then
    C. Press the down arrow to reach the "Fundamental Meter" selection, then
    D. Press ENT to reach the "Meter Sub Menu," then
    E. Press ENT to reach the "Fundamental Line Meter" to observe volts and amps, then
    F. Press the down arrow three times to view P.
    Pressing ENT several times will take you back to the "Rotating Display"
13. View the Pearson Coil waveform. Expect something like this. It is actually very "clean" for an inverter (about 20% THDI)

Save screen snapshot #1
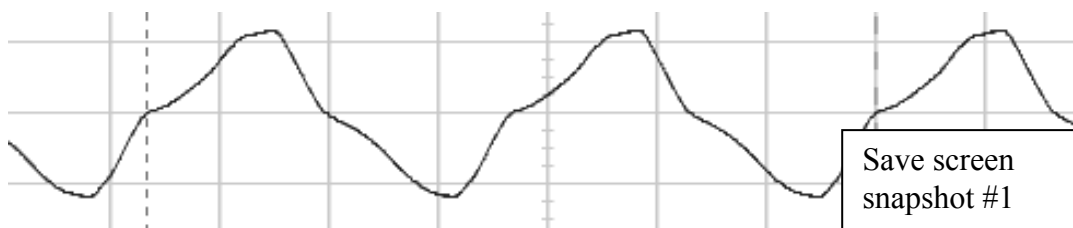
14. Open the Shorting knife-switch, and then the On/Off knife-switch
15. Turn down the variac, and then switch off the variac.

If you want to send solar power to the grid, use the solar interface circuit and one-half of the 25Vac transformer winding.