

“An Overview of Transistor Modeling for RF and Microwave Applications”

by Dr. Charles Baylis

Assistant Professor, Wireless and Microwave Circuits and Systems (WMCS) Program,

Department of Electrical and Computer Engineering, Baylor University

ABSTRACT

This presentation discusses the role of transistor modeling in the microwave circuit design cycle and provides an overview of model extraction procedures. Microwave transistor models are extracted from current-voltage (IV), S-parameter, and nonlinear power measurement data. Following a discussion of this procedure, some challenges that arise in modeling are then addressed. Special focus is given to thermal and trapping issues that can be encountered in the device during measurements, potentially causing inaccuracy in the models extracted from these measurements. Methods for diagnosing and properly modeling these effects are discussed, including the use of pulsed IV and pulsed S-parameter measurements. A bias-dependent modeling approach developed by the speaker that provides for accurate thermal and trapping dependence of wide-bandgap devices is briefly surveyed.

BIO

Charles Baylis is an Assistant Professor in the Department of Electrical and Computer Engineering at Baylor University in Waco, Texas. He received the B.S.E.E., M.S.E.E., and Ph.D. degrees from the University of South Florida in 2002, 2004, and 2007, respectively. Dr. Baylis served as a Visiting Assistant Professor at USF from 2007-2008 and joined the Baylor faculty in August 2008. Along with Dr. Randall Jean, he directs the Wireless and Microwave Circuits and Systems (WMCS) program at Baylor. His present research interests include RF active circuit design (power amplifiers, oscillators, frequency multipliers, etc.), microwave transistor modeling, mathematical analysis of engineering problems, and biological applications of RF and microwave measurements and technology. He has authored several papers related to his areas of interest. Some of his recent accomplishments include the development of an algorithm to perform more efficient load-pull measurements and devising a method to model FET trapping effects based on the quiescent operating point.