Design and Control of a Grid-Connected Three-Phase 3-Level NPC Inverter for Building Integrated Photovoltaic Systems

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Abstract-- **This paper presents the design and control of a grid-connected three-phase 3-level Neutral Point Clamped (NPC) inverter for Building Integrated Photovoltaic (BIPV) systems. The system consists of a PV array, boost DC/DC converter, 3-level NPC inverter, LC filter and the grid. The 3-level NPC inverter is designed without a galvanic isolation transformer and its current controller is developed to minimize leakage currents though common-mode voltage loops in the PV systems. A prototype 13kW NPC inverter with a LC filter was fabricated and tested, resulting in a low total harmonics distortion (THD) of less than 3% THD and 97.5% efficiency at the peak load. The detail simulation and test results are discussed.**

Index Terms **– A transformerless 3-level NPC inverter, PV inverter, current control, LC filter, BIPV.**

I. Introduction

Recently, various photovoltaic (PV) systems have been developed and widely installed for renewable energy generation. Small-sale PV systems of up to 15kW are emerging in the market of building integrated photovoltaic (BIPV) systems [1]. These systems typically require a galvanic isolated three-phase inverter that converts DC voltage from PV arrays into AC voltage and feeds it into utility grid. The inverter with galvanic isolation can provide solutions for safety concerns and voltage and current scalability, but they can be quite heavy and very expensive. Furthermore, line transformers and high frequency transformers cause additional losses in the power conversion circuit which cause the PV inverters to have poor overall efficiency [2].

A transformerless inverter topology is an alternative solution to overcome the aforementioned limitation. However, there are compatibility problems that have been found in common-mode voltage and leakage current resulting in safety and electromagnetic interference (EMI) issues. Although these problems are generic to the single-phase inverter with high-speed switching, their effects are magnified by high switching frequencies [3]. In fact, high-speed switching induced *dv/dt* and *di/dt* causing many of the compatibility problems.

The same problems are seen in the three-phase inverter system. Thus, the design should have two goals. One, to lower *dv/dt* and *di/dt* to protect the PV array and extend the life cycle of dc link capacitor and another, to decrease the leakage current through the common-mode paths between the PV array and the grid. The design should also reduce EMI. Two main questions to ask are (1) how to lower the *dv/dt* and *di/dt* and (2) how to optimize the PWM switching strategies of the inverter and the boost DC/DC converter.

A multilevel inverter topology offers a solution to reduce *dv/dt* voltage stress across each device by increasing the number of levels. It is also possible to have lower voltage rating in DC link capacitors, resulting in a greater number of choices for low cost capacitors [4]. Furthermore, with advanced switching modulation strategies the PV systems can eliminate the leakage current though common-mode voltage loops [5].

In this paper, a three-phase 3-level diode clamped based neutral point clamped (NPC) inverter with LC filter is proposed for BIPV systems. The inverter is newly designed and controlled by the proposed current controller for the effective active and reactive power controls. The new current controller of the inverter with LC filter is also designed to reduce the total harmonics distortion (THD) to be less than 5%. Various simulations are performed with PSIM simulation software and MATLAB to characterize the common-mode voltage and the leakage current and to design the current controller and the LC filter. For validation, a prototype 13kW three-phase 3-level NPC inverter is fabricated and tested.

II. Photovoltaic Three-Phase 3-Level Inverter System

A. Overall System Configuration

Fig. 1 shows the overall configuration of a transformerless three-phase 3-level NPC inverter system. The system consists of a PV array, boost DC/DC converter, 3-level NPC inverter, LC filter and the grid. The output voltage of the PV array is widely varying from 350V to 850VDC. For the utility grid, the output of the inverter system is defined as a 13kW, 380V, 60Hz. To achieve high system efficiency, low switching frequencies are chosen. The switching frequency of the DC/DC converter is selected to be 10 kHz and the switching frequency of the inverter is selected to be 5 kHz.

The 3-level NPC inverter can produce five voltage levels on the utility grid; V_{dc}, $+V_{dc}/2$, 0, $-V_{dc}/2$, and $-V_{dc}$ depending on the switching frequency. A LC filter is employed to reduce the voltage ripple, resulting in the low THD.

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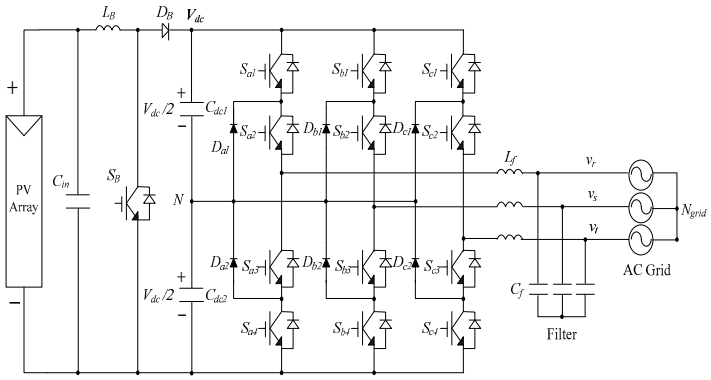


Fig. 1. Overall configuration of a transformerless three-phase 3-level NPC inverter system.

B. PWM Strategy

Since the PV array has an existing galvanic connection between the ground of the grid and the PV array, the common-mode voltage loop can form a resonant circuit with the stray capacitances and leakage inductance during zero-sequence switching states [5-6]. Such a direct tie or low impedance tie from the PV array and the grid will allow zero-sequence current flow and cause triple harmonic currents into the inverter through the PV modules, the ground, and the DC and AC filter elements. Furthermore, when a varying common-mode voltage that is the voltage common to both input PV array and output grid terminals can stimulate the resonant circuit, it may generate high common-mode current on the inverter. Thus, this should be avoided because the system may become unstable.

Three alternative PWM strategies are available for the three-phase NPC inverters; 1) Alternative phase opposition disposition (APOD), 2) Phase opposition disposition (POD), and 3) Phase disposition (PD).

Fig. 2 shows the PD PWM switching pattern of the one-leg in the 3-level NPC inverter using phase disposition method. The selected PD strategy can achieve the lowest harmonic distortion for the line-to-line voltage of the inverter [6]. Considering the system efficiency, the switching frequency of the DC/DC converter is selected for 10 kHz to reduce the input current ripple, and 5 kHz for the inverter switching frequency. The third harmonic injection PWM with two carriers-based switching is programmed by using DSP TMS320F2812.

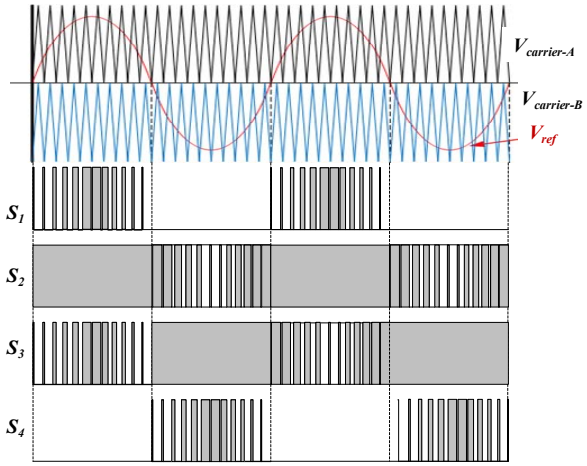


Fig. 2. PD PWM switching pattern of one 3- level inverter phase-leg.

II. Control and Design of Three-Phase 3-Level NPC Inverter with LC Filter

A. Control System

A control system of a grid connected three-phase 3-level NPC inverter system as shown in Fig. 3 consists of two main controllers; the DC-side controller for the boost DC/DC converter, and AC-side controller for the inverter. These controllers are incorporated with the overall system controller in the inverter circuit that is regulated with the DC link voltage, the line-voltage at the point of common coupling (PCC), the inverter current and the grid current.

The DC/DC converter is controlled to maintain the fixed DC link voltage enough high to make the inverter operate. To achieve the maximum power from the PV array, a perturbation and observation (P&O) method is applied for the maximum power point tracking (MPPT) controller [7]. The output of MPPT generates current reference of the boost inductor current. Both voltage controller for MPPT and inductor current controller use PI controller in this system.

The control of the 3-level NPC inverter is to regulate DC voltage and supply power generated by PV array to the grid with low harmonic currents. The current controller is implemented in the *d-q* synchronous frame and its manipulated variables are generated in the *d-q* coordinate system. Due to the fact that phase quantities are required in the PWM switching pattern, PI controller results are transformed back to the *αβ* coordinate system and then back into phase quantities [8].

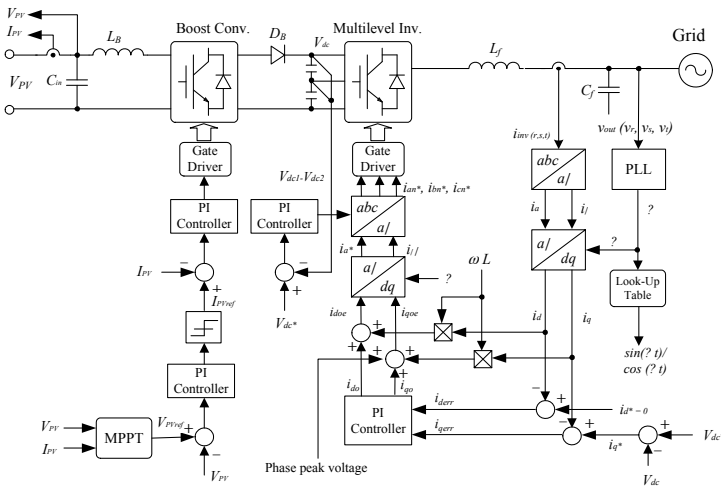


Fig. 3. Control block diagram of a 3- level NPC inverter system.

B. Current Control

The current controller is designed with two control loops for active and reactive power controls [9]. The current controller is used to regulate the output power of the PV system. Each current loop with a proportional-integral (PI) controller regulates the output current to follow its reference values.

To control the active power, the inverter output power is measured and compared to the power reference. The power error feeds a PI controller having a current reference, i_q^*, as

output. To have the *d*-axis current reference, i_d^*, the inverter output voltage also is measured and compared to the voltage reference. In the same way, the error feeds to a PI current controller and is regulated for reactive power by the grid-connected inverter. The controller output power is controlled by the measured output power of the inverter and the reference active power. All PI controller gains are determined by the input error between the measured and the reference voltages.

On the other hand, the current reference designed with a synchronous reference *d-q* axis frame is oriented to the *d*-axis rotating at the grid frequency. The measured three phase voltages are transformed to the synchronous rotating reference at the grid frequency. And the output of this PI controller is used to generate the current commands for the inverter switching. The *d-q* current command components, i_d^* and i_q^* are transferred to the *a-b-c* current command components, i_{an*}, i_{bn*} and i_{cn*}, respectively. All gate signals are produced by these reference vectors synthesized by space vector modulation (SVM) algorithm.

The PI current controller $G_{PI}(s)$ in the *d-q* reference frame is defined as:

$$G_{PI}(s) = K_P + \frac{K_i}{s} \tag{2}$$

where, K_p is the proportional gain, and K_i is the integral constant. Since the PI controller is decomposed into a parallel structure and the K_p, is time invariant, the gain parameters are ineffective on the direct and inverse sequence components of the current error [10]. Thus, the K_P should be interpreted as the sum of the proportional gains of the current sequence controller. For this, the PI controller requires a grid voltage feed-forward loop for the dynamic response. However, this approach may result in poor THD of the load current.

B. LC Filter

A simple L-filter is widely used for the inverter to reduce the current harmonics. The L filter should be designed with line frequency, so that it requires high inductance value, resulting in cost rising in the order of several kilowatts [11]. In additions, the dynamic response may become poor. Thus, LC or LCL filters consisting of quite small values of inductor and capacitor can replace the low pass filter. The LCL filter needs more space and cost because of two inductors. The efficiency, cost, losses, weight and size are different, depending of the filter type. In this work, an LC filter is designed.

In order to design the LC filter [12-13], firstly the maximum ac current ripple should be defined. In this design, the inverter side inductance is selected with 5% of the phase current at rated power. Based on this guideline, the fundamental component of grid current is assumed to be zero. Then, the fundamental component of the filter inductor voltage is to be also zero. Thus the voltage across the inductor is defined as:

$$V_L = V_{inv} - V_g \tag{1}$$

where V_L is the inductor voltage, V_{inv} is the inverter output voltage and V_g is the grid voltage.

On the other hand, the phase voltage of the 3-level inverter has five levels to the mid-point: V_{dc}, $V_{dc}/2$, 0, $-V_{dc}/2$, and $-V_{dc}$. The phase voltage depends on the switching frequency f_s that is higher than the grid frequency f_N. Thus, the time average value of the inverter output voltage V_{av} can be defined as constant during the switching time T_s. In this case, the peak-to-peak value of the filter inductor current when using PD PWM switching method is also obtained as:

$$\Delta I_{pp} = 2I_{rpm} = \frac{\frac{V_{dc}}{2} - V_{av}}{L_f} \cdot \frac{d_1}{f_s} \tag{2}$$

where, I_{pp} and I_{rpm} are the peak-to-peak value and maximum value of filter inductor current ripple, respectively. L is the filter inductance value, d_1 is the duty cycle. During the interval of $0 < \omega t < \pi$,

$$V_{av}(\omega t) = d_1(\omega t)\frac{V_{dc}}{2} \tag{3}$$

$$d_1(\omega t) = m_a \sin(\omega t) \tag{4}$$

where, m_a is modulation index. Hence, the maximum inductor current ripple I_{rpm} can be expressed as follows:

$$\begin{aligned} I_{rpm} &= \frac{V_{dc}}{4L_f f_s}\left[1 - d_1(\omega t)\right]d_1(\omega t) \\ &= \frac{V_{dc}}{4L_f f_s}\left[1 - m_a \sin(\omega t)\right]m_a \sin(\omega t) \end{aligned} \tag{5}$$

Assuming $m_a = 1$, the maximum value of I_{rpm} is 1/4 at π/6, 5 π /6.

$$L_f = \frac{V_{dc}}{16 \cdot f_s \cdot \Delta I_{ph(\max)}} \tag{6}$$

Thus, based on switching frequency, the value of the inverter- side inductor was selected.

For the selection of the filter capacitance, it is considered that the maximum power factor variation seen by the grid should be set to 5%. From the capacitance variation, the overall system impedance base value, Z_B, is calculated as:

$$Z_B = \frac{v_G^2}{P_{Av}/3} \tag{7}$$

$$C_B = \frac{1}{\omega_N \cdot Z_B} = \frac{1}{2\pi f_N \cdot Z_B} \tag{8}$$

$$C_{\max} = 0.05 \cdot C_B \tag{9}$$

where, v_G is the line-to-line rms voltage, P_{Av} is the rated active power, and ω_N is the grid frequency. In (9), while using values higher than this 5%, the power factor of the system will be less than the power factor expected. That is, if too large capacitors are selected, the inductor current ripple will be increased.

On the other hand, since the transformerless inverter has the common-mode voltage loops during PWM switching, the resonance circuit is formed and its resonant frequency will be

calculated under the boundary condition between the switching frequency and the control bandwidth [14]:

$$10 \cdot f_N \le f_{res} \le \frac{f_S}{2} \tag{10}$$

where, f_{res} is the resonance frequency and is defined as:

$$f_{res} = \frac{1}{2\pi\sqrt{L_f C_f}} \tag{11}$$

It is clear that the selection of the switching frequency should be far above the resonant frequency of the LC filter.

III. Simulation and Verification

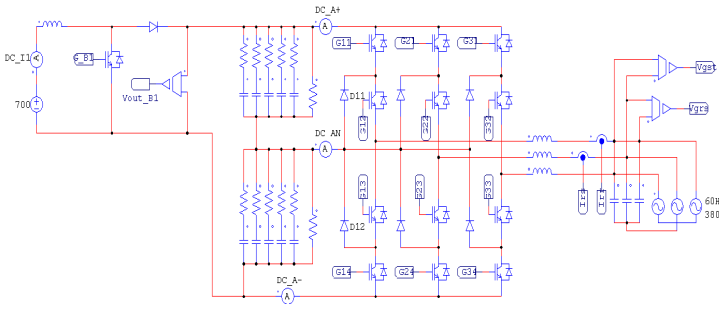
C. Digital Simulation Setup

For effective system evaluations, the proposed inverter is simulated using PSIM. Table 1 shows System parameters for simulation. Fig. 4(a) shows a PSIM based schematic diagram and Fig. 4(b) shows the 3-level inverter output voltage and line-to-line grid voltage waveforms. It can be seen that the inverter output voltage of the 3-level inverter has five voltage levels, V_{dc}, $V_{dc}/2$, 0, $-V_{dc}/2$, and $-V_{dc}$, depending on the switching frequency. Fig. 4(c) shows the injected rated currents to the grid. The simulation result shows that the injected currents are sinusoidal and THD of current achieves about 2.5%.

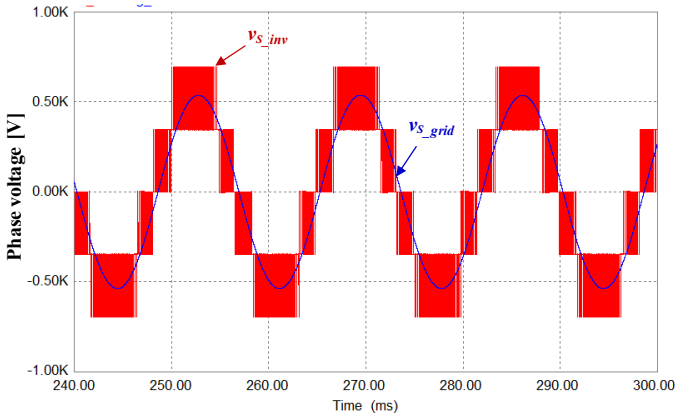
Fig. 5 shows the Bode plots of the LC filter which can be seen that at low frequency when the damped LCL filter behaves like an L filter of the same value. The figure also shows the difference among four different types of filters: L, LC and LCL with no damping resistor, and LCL with damping resistor. As shown, the -40dB attenuation is obtained from the LC filter. Thus, the grid-side current ripple is highly attenuated under the grid impedance variation.

TABLE I
Simulation Parameters

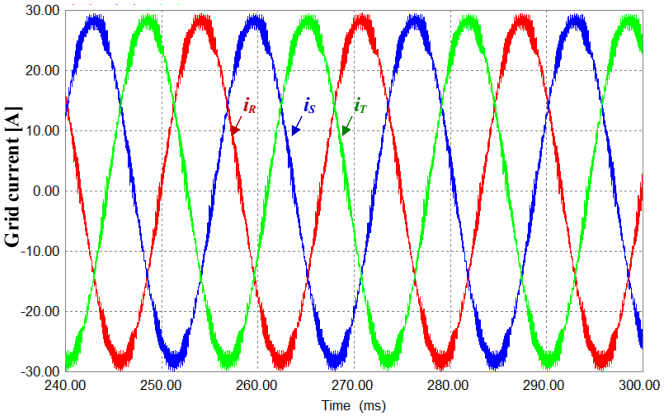
Key parameters	Values
PV Array voltage	350 - 850 V_{dc}
Grid	60Hz, 3Φ, 380 $V_{(LL)}$
Nominal Power	13kW
PWM carrier frequency	
- Inverter	5 kHz
- DC-DC converter	10 kHz
LC Filter	4.5mH/ 10μF



(a) PSIM simulation schematic diagram.



(b) Grid voltage and 3-level PWM output voltage.



(c) Injected current to the grid (*Ir, Is, It*).

Fig. 4. PSIM based schematic diagram and simulation output.

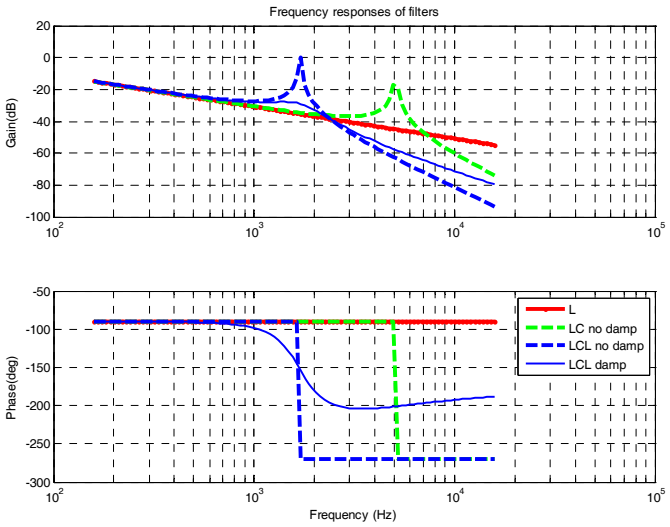


Fig. 5. Bode plots of the LC filter.

Fig. 6 shows the current and voltage waveforms between PV terminals and the ground. Equivalent parasitic capacitors, 90.04nF, are connected to the +, - terminals of the 13kW PV array. The leakage current to the ground is below 3mA, low enough to not be an electric shock hazard even though there the loss balancing control is not good. The capacitor voltages only have low frequency ripple.

From the result of simulation, it is clear that the 3-level NPC inverter is a good choice for the transformerless PV inverters. Even though the NPC inverter has a low switching frequency and a LC filter, the THD and power quality meets the requirement of IEEE Standards. And safety is also achieved without transformer.

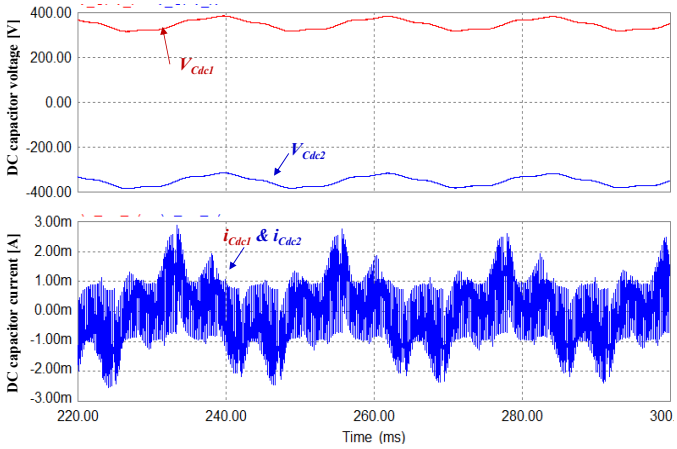


Fig. 6. Voltages (top) and currents (bottom) of the parasitic capacitors between PV terminals and the ground.

IV. Experimental Results

The overall system of grid-connected NPC 13kW inverter, as shown in Fig. 7, is implemented fully in software adopting a 32-bit fixed-point DSP TMS320F2812. The inverter controller is implemented in software, and the PWM pulses are generated through the internal pulse generator of the DSP. Voltage and current signals are measured by using the 12-bit resolution of internal analog-to-digital (A/D) converter in the DSP. Also a four-channel 8-bit digital-to-analog (D/A) converter has been used for debugging. In addition, experimental comparisons with the conventional full-bridge inverter with transformer have been carried out. Both systems have used DSP TMS320F2812 control boards and the same control algorithm. But, two different PI gains are selected to optimize the desired responses.

However, the conventional full-bridge inverter has 10 kHz switching frequency but the NPC inverter has 5 kHz. The power devices are Vincotech's IGBT 600V-65A for the NPV inverter.

Fig. 8 shows the experimental three-level PWM inverter output voltage waveforms on the three phase voltages, v_R,v_S, and v_T. Fig. 9 shows the experimental grid waveforms on the rated inverter output currents, i_R, i_S, and i_T. As presented, the proposed inverter system with LC filter operates well with the current controller.

Fig. 10 (a) and (b) show system efficiency and current THD measured by the WT1600 digital meter. It is clear that both inverters achieve a lower THD to meet the requirements to interface the grid networks. The transformerless NPC multilevel inverter has better efficiency than the conventional inverter, because of the lower switching loss and the lack of transformer loss. It is clear that the proposed 3-level NPC inverter achieved 97.5 % efficiency over a wide range of loads and it improved 4% higher than the conventional two-level inverter with transformer. In the THD comparisons, the proposed inverter also achieved the equal performance in power quality even though it has lower switching frequency.

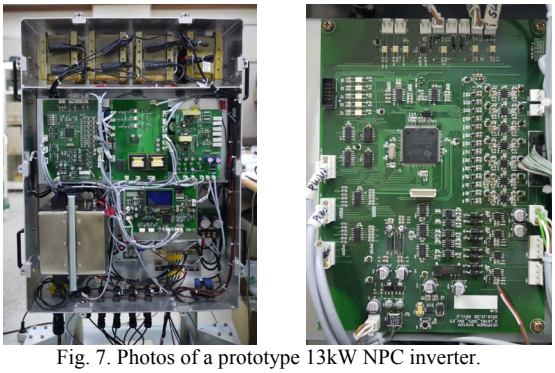


Fig. 7. Photos of a prototype 13kW NPC inverter.

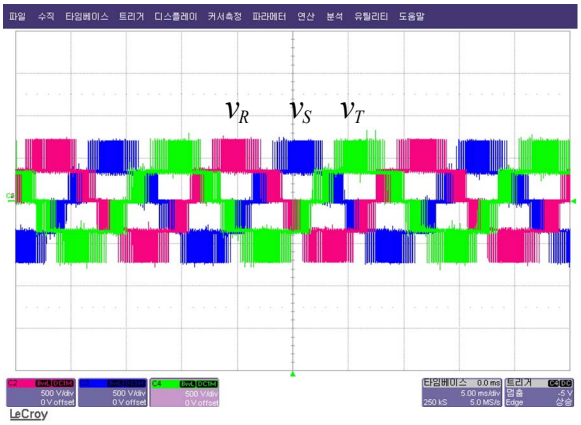


Fig. 8. Experimental three-level NPC inverter output voltage waveforms (v_R,v_S, and v_T)

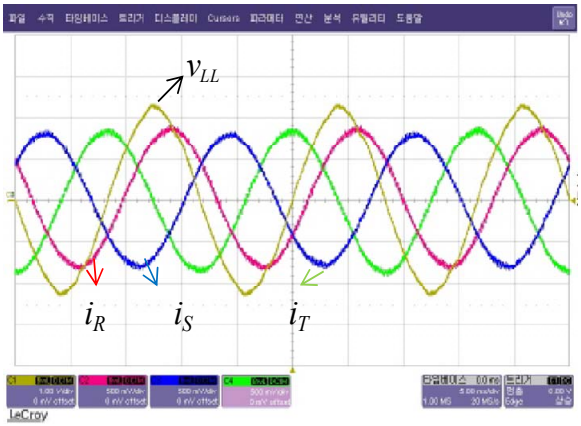
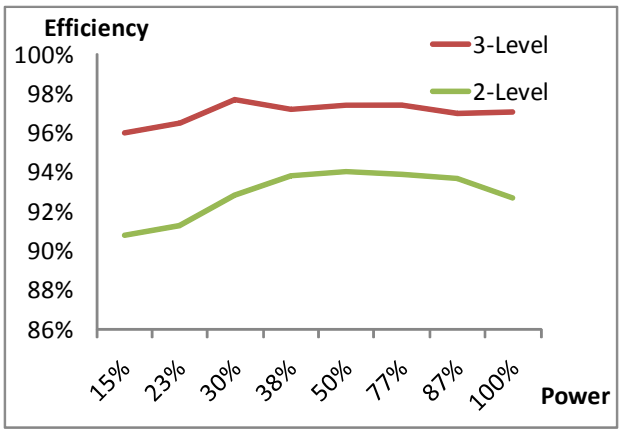
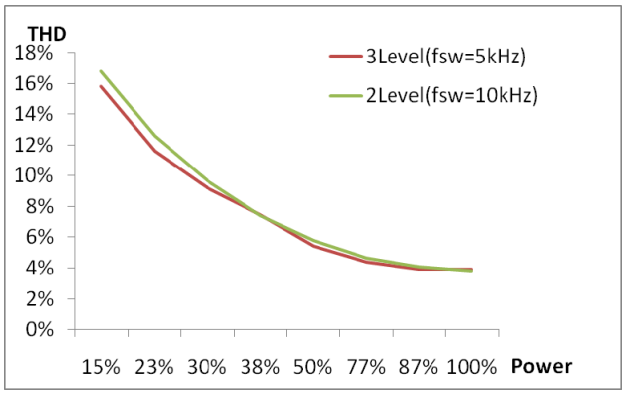


Fig. 9. Experimental waveforms of grid voltage V_{LL} and current i_R, i_S, i_T at rated output.

Fig. 11 shows the emission noise of AC output that is measured from 150kHz to 30MHz. This result meets the requirement of IEC 61000-6-4 that the interference voltage requires a 79 dB (μV) at 150kZ, average 60 dB (μV) at 30MHz and shows 57.61dB at150kHz, flat low at the entire frequencies. As can seen in Fig. 11, the leakage current through common-mode voltage loops in the PV system during zero-state sequences is almost eliminated by using PD PWM switching method.



(a) Comparison of efficiencies.



(b) Comparison of THDs of injected current to the grid.

Fig. 10. Comparison of efficiencies and THDs between transformerless 3- level NPC inverter and 2-level inverter with transformer.

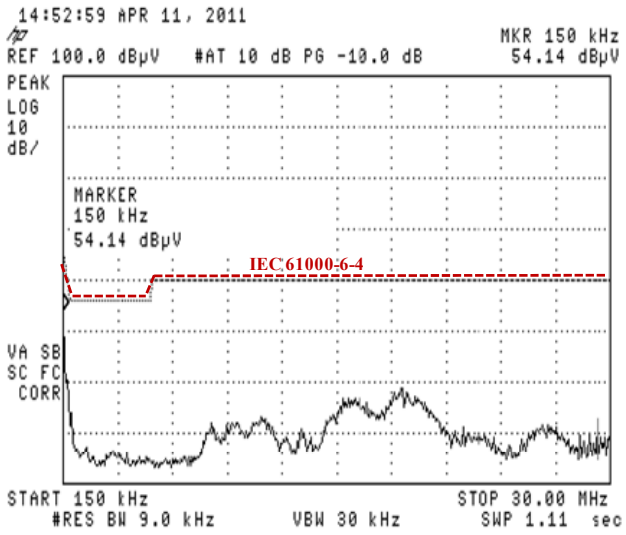


Fig. 11. Conducted noise measurement of the proposed inverter system.

V. Conclusions

This paper presented the design and control of a transformerless grid-connected three-phase 3-level NPC inverter for BIPV systems. The proposed inverter was also characterized and analyzed for the effective grid interface. In addition, a new current controller using PI control was designed and fully implemented in software for active and reactive power control.

Various simulations were performed with PSIM simulation software and MATLAB to characterize the leakage current through common-mode voltage loops in the PV system. A phase disposition (PD) pulse-width-modulation (PWM) switching strategy was applied to the inverter so that the leakage current through the common-mode voltage loops was reduced, resulting in the reduction of emission noises. A prototype 13kW NPC inverter with LC filter demonstrated a low total harmonics distortion (THD) of less than 3% THD and 97.5% efficiency at the peak load.

As a result, it concluded that the proposed transformerless 3-level NPC inverter with LC filter can be utilized to eliminate common-mode voltage and the leakage current. The result is a cost effective solution for small-scale PV systems of up to 15kW for building integrated photovoltaic (BIPV) systems.

References

[1] T. Kerekes, R. Teodorescu, and U. Borup, "Transformerless Photovoltaic Inverters Connected to the Grid," *IEEE 2007 Applied Power Electronics Conference, (APEC)*, 2007, pp. 1733-1737.

[2] P. Zacharias and B. Burger, "Overview of Recent Inverter Developments for Grid-Connected PV Systems," in *21st European Photovoltaic Solar Conference*, 2006, Dresden, Germany.

[3] T. Kerekes, R. Teodorescu, and M. Liserre, "Common mode Voltage in case of Transformerless PV inverters connected to the Grid," *IEEE 2008 International Symposium on Industrial Electronics (ISIE)*, 2008, pp. 2390-2395.

[4] B. M. Song and J. S. Lai, "A multilevel soft-switching inverter with inductor coupling," *IEEE Trans. Ind. Appli.*, vol. 37, pp. 628-636, Mar./Apr. 2001.

[5] B. P. McGrath and D. G. Holmes, "A comparison of multicarrier PWM strategies for cascaded and neutral point clamped multilevel inverters," *IEEE 31st Annual Power Electronics Specialists Conference (PESC'00)*, June 2000, pp. 674-679.

[6] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, "A New Multilevel PWM Method: A Theoretical Analysis," in *IEEE Transactions on Power Electronics*, vol. 7, no. 3, pp.497- 505, July 1992.

[7] B. M. Song, Y. Kim, H. Cha, and H. Ree, "Current Harmonic Minimization of a Grid-Connected Photovoltaic 500kW Three-Phase Inverter using PR Control," *IEEE 2011 Energy Conversion Conferences and Exposition (ECCE 2011)*, Phoenix, AZ, Sept. 2011.

[8] F. Blaabjerg, R. Teodrescu, M. Liserre, and A. V. Timbus, "Overview of Control and Grid Synchronization for Distributed Power Generation Systems," in *IEEE Trans. on Industrial Elect.*, vol. 53, no.5, pp. 1398 – 1409, Oct. 2006.

[9] H. R. Seo, M. Park, I. K. Yu, and B. M. Song, "Performance Analysis and Evaluation of a Multifunctional Grid-Connected PV System using Power Hardware-in-the-Loop Simulation," *IEEE 2011 Applied Power Electronics Conference (APEC 2011)*, March 2011, pp. 1945-1948.

[10] E. Cengelci, S. U. Sulistijo, B. O. Woom, P. Enjeti, R. Teodorescu, and F. Blaabjerg, "A New Medium Voltage PWM Inverter Topology for Adjustable Speed Drives," in *Conf. Rec. IEEE-IAS Annu. Meeting,* St. Louis, MO, Oct. 1998, pp. 1416-1423.

[11] M. Liserre, F. Blaabjerg, and S. Hansen, "Design and Control of an LCL filter based Three-Phase Active Rectifier," in *IEEE Transactions on Industry Applications*, vol. 41, no.5, pp. 1281 – 1291, sep./Oct. 2005.

[12] E. Twining and D. G. Holmes, "Grid Current Regulation of a Three Phase Voltage Source Inverter with an LCL Input Filter," in *IEEE Transactions on Power Electronics*, vol. 18, no. 3, pp. 888-895, May 2003.

[13] K. H. Ahmed, S. J. Finney, and B. W. Williams, "Passive Filter Design for Three-Phase Inverter Interfacing in Distribution Generation," *Journal of Compatibility in Power Electronics (CPE'07),* vol. 12, no.2, pp. 1-9, May/June 2007.

[14] H. Kim and K. H. Kim, "Filter design for grid connected PV inverters," *IEEE International Conference on Sustainable Energy Technologies (ICSET'08)*, pp. 1070-1075, 2008.

VI. BIOGRAPHIES

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