

# ELC4438: Embedded System Design

## ARM Embedded Processor

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# Intro to ARM Embedded Processor

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- (UK 1990) Advanced RISC Machines (ARM) Holding
- Produce IP core and license to semiconductor companies
  - produce embedded MPU and MCU according to company strength
  - In electronic design a semiconductor intellectual property **core**, **IP core**, or **IP** block is a reusable unit of logic, cell, or chip layout design that is the intellectual property of one party. **IP** cores may be licensed to another party or can be owned and used by a single party alone.
- Semiconductor companies, e.g. TI, Samsung, Freescale, NXP, ST Semiconductor

# ARM Embedded System Support

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- Windows CE  
(Compact/Consumer/Connectivity/Companion – Electronics)
- $\mu$ Clinux (from Linux 2.0/2.4)
- pSOS
- VxWorks (US WindRiver 1983 realtime OS, used in F-16, FA-18, B-2, Patriot SAM, Pathfinder, etc.)
- $\mu$ C/OS (open source, mostly C coded)
- Palm OS
- Windows 8

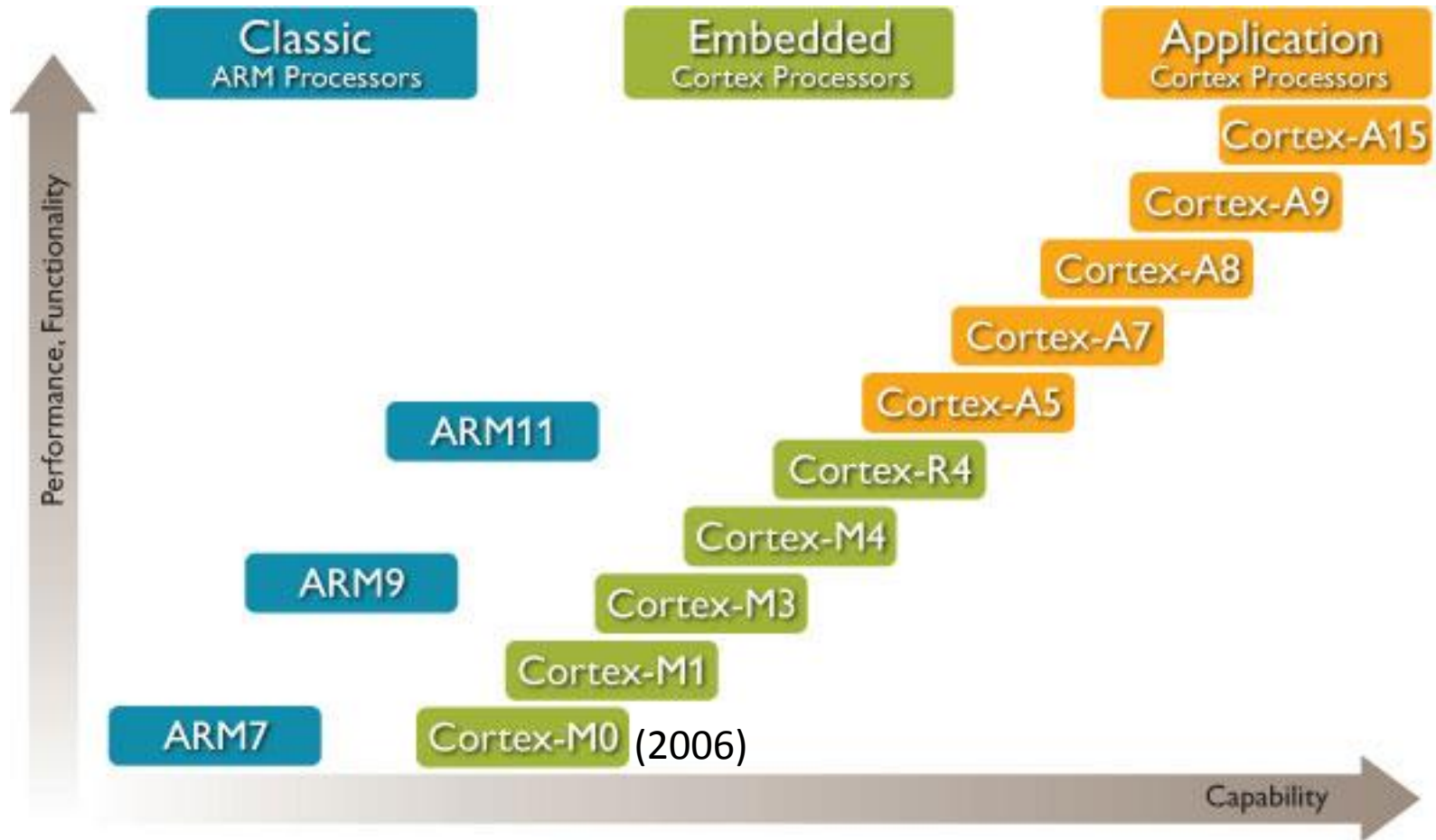
# ARM Processor Feature

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Typical RISC Feature:

- Small volume, low power, low cost, high performance
- Use many registers, fast execution time of instructions
- Easy addressing methods, high-efficiency
- Most data operations done in registers
- 32-bit wordlength
- Embedded online simulator included

# ARM Processor Series



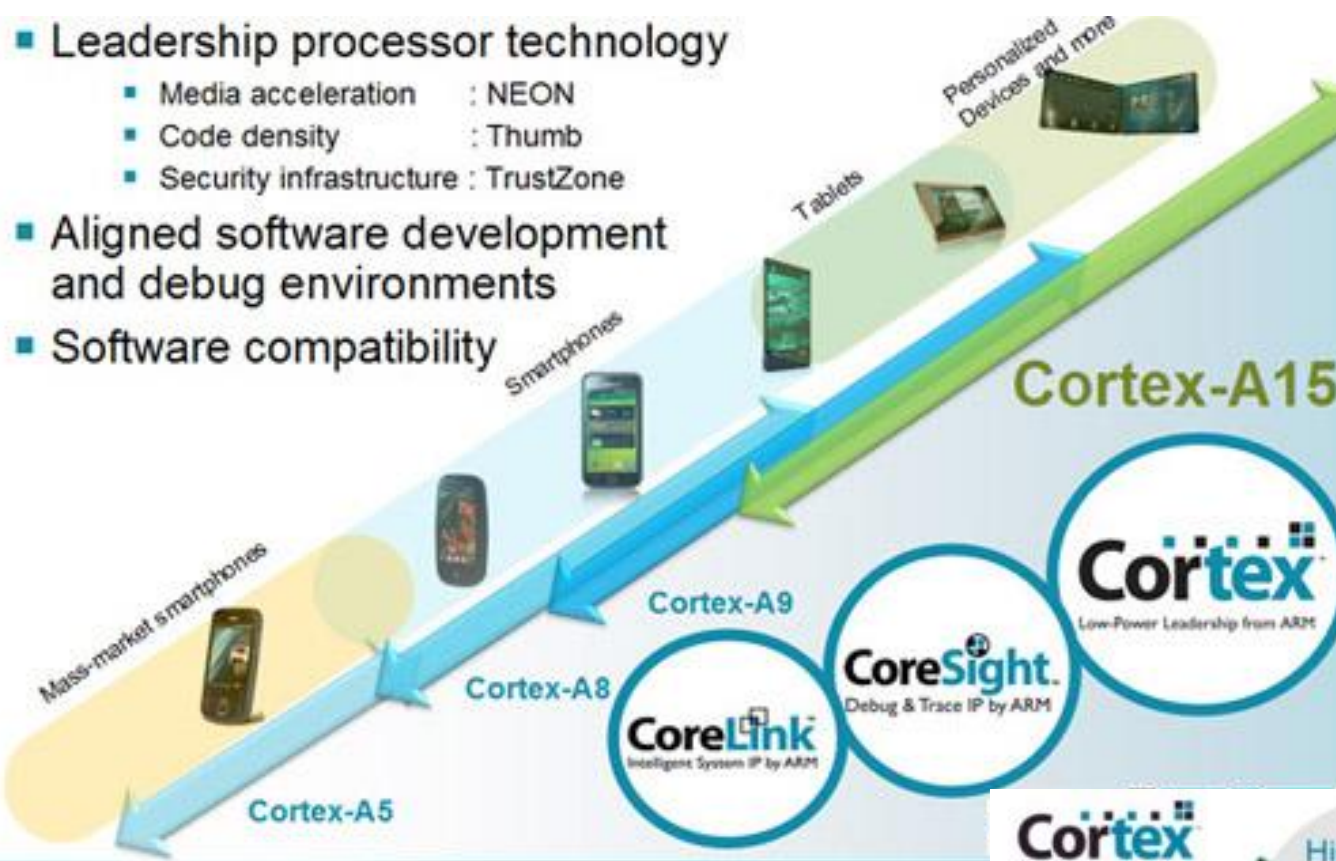
- ARM [x] [y] [z] [T] [D] [M] [I] [E] [J] [F] [-S]
  - [x] series number ARM7, ARM9
  - [y] memory storage and protection ARM72
  - [z] high-speed buffer ARM720, ARM940
  - [T] Thumb instruction set
  - [D] Support JTAG online/on-chip testing
  - [M] Hardware Multiplier
  - [I] Embedded ICE Macrocell
  - [E] Enhanced DSP instructions
  - [J] Java accelerator Jazelle
  - [F] Floating point
  - [S] Source code, can be applied to EDA (Electronic Design Automation)

■ Leadership processor technology

- Media acceleration : NEON
- Code density : Thumb
- Security infrastructure : TrustZone

■ Aligned software development and debug environments

■ Software compatibility



**Cortex-R4 (2006)**

- High-performance, real-time
- Deterministic interrupts
- Feature set configurable
- Dependable systems

**Cortex-R5 (2011)**

- Performance enhancing features
- Fast peripheral access
- I/O coherency
- Dual core configuration
- Extended error management
- Space-saving FPU

**Cortex-R7 (2011)**

- Large performance increase
- Advanced microarchitecture
- Higher clock frequency
- Quality of Service features
- Symmetric Multi-Processing
- Twin core and I/O coherency
- Extended real-time memory
- Hard error management
- Integrated interrupt controller

# ARM Cortex

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- ARM Cortex-A: Consumer Entertainment Electronics, Wireless Product
  - Cortex-A9/A10 dual-core quad-core 1GHz
  - Cortex-A15 quad-core 2.5GHz
- ARM Cortex-A8 1 GHz
  - Sophisticated pipelining
  - Thumb-2 instruction set (32-bit and 16-bit)
  - NEON™ signal processing – H.264, MP3
  - Jazelle-RCT Java accelerator
  - JIT (Just in Time) and DAC (Dynamic Adaptive Compilation) Technologies
  - e.g. iPad, iPhone4 A4 processor is Cortex-A8 manufactured by Samsung



- The implementation of the Advanced SIMD (Single Instruction, Multiple Data) extension used in ARM processors is called NEON
- SIMD technology uses a single instruction to perform the same operation in parallel on multiple data elements of the same type and size

# ARM® Cortex®-A Current Portfolio

Q4 2015

## Cortex-A15

High-performance with infrastructure feature set



## Cortex-A17

High-performance with lower power and smaller area relative to Cortex-A15



## Cortex-A57

Proven high-performance 64/32 bit CPU



## Cortex-A72

Highest performance 64/32 bit CPU



High Performance

## Cortex-A9

Well established mid-range processor used in many markets

## Cortex-A53

Balanced performance and efficiency 64/32 bit CPU



High Efficiency

## Cortex-A5

Smallest and lowest power, optimized for single-core

## Cortex-A7

Most efficient ARMv7-A, higher performance than Cortex-A5



## Cortex-A35

Highest efficiency 64/32 bit CPU



Ultra High Efficiency

© ARM 2015

ARMv7-A

Key: big.LITTLE compatible

ARMv8-A

ARM

# ARM® Cortex®-R and Cortex-M Processor Portfolio

Q4 2015

## Cortex-R4

Real-time  
standard

## Cortex-R5

Functional safety

## Cortex-R7

High  
performance  
4G modem and  
storage

Cortex-R

## Cortex-M0

Lowest cost,  
low power

## Cortex-M0+

Highest energy  
efficiency

## Cortex-M3

Performance  
efficiency

## Cortex-M4

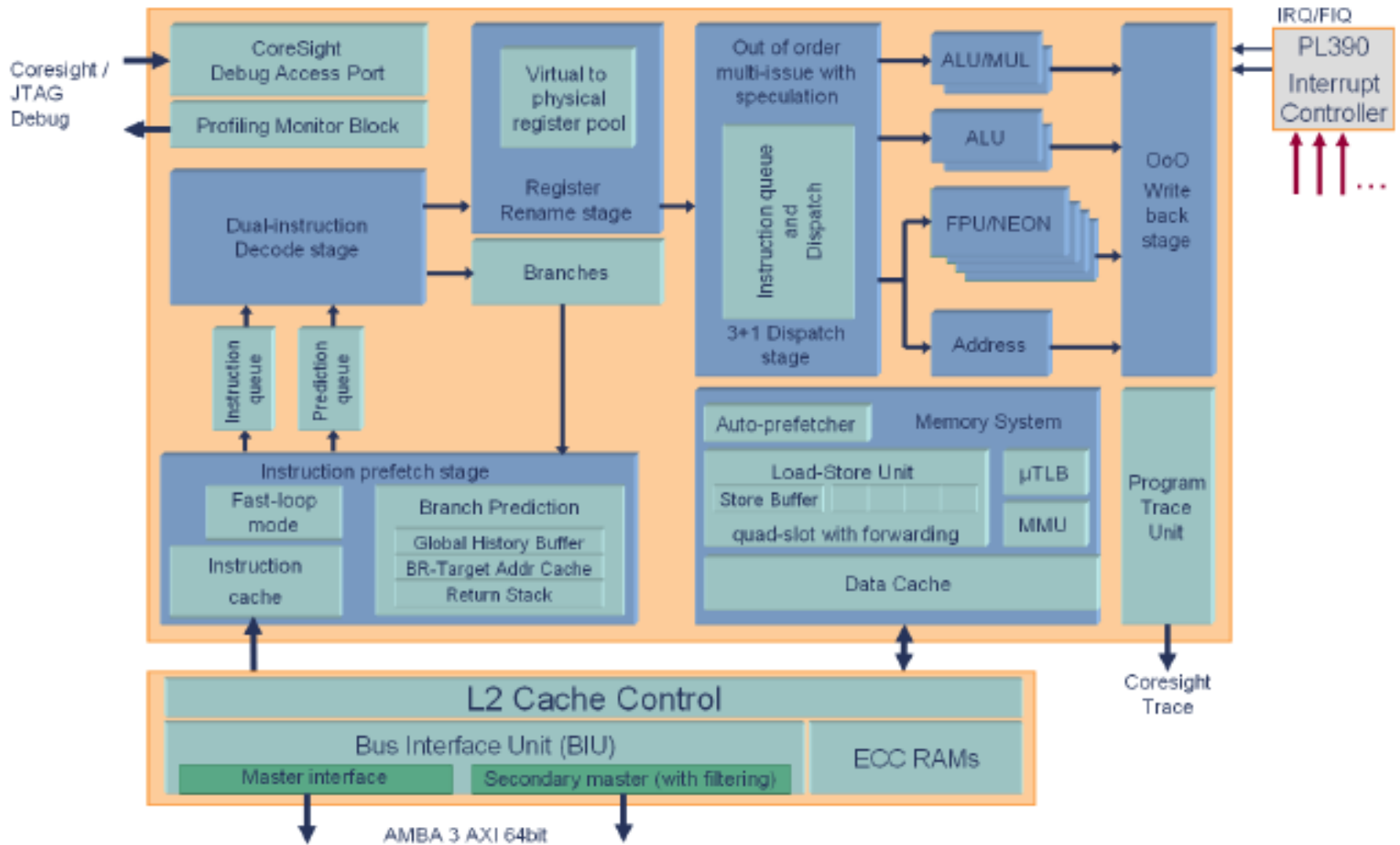
Mainstream  
control & DSP

## Cortex-M7

Maximum  
performance  
control & DSP

Cortex-M

# ARM Cortex-A8/A9



# ARM<sup>®</sup> Cortex<sup>®</sup>-A8

ARM CoreSight<sup>™</sup> Debug and Trace

ARMv7  
32b CPU

NEON<sup>™</sup>  
Data Engine

Floating Point  
Unit

16-32k  
L1 Instruction Cache

16-32k  
L1 Data Cache

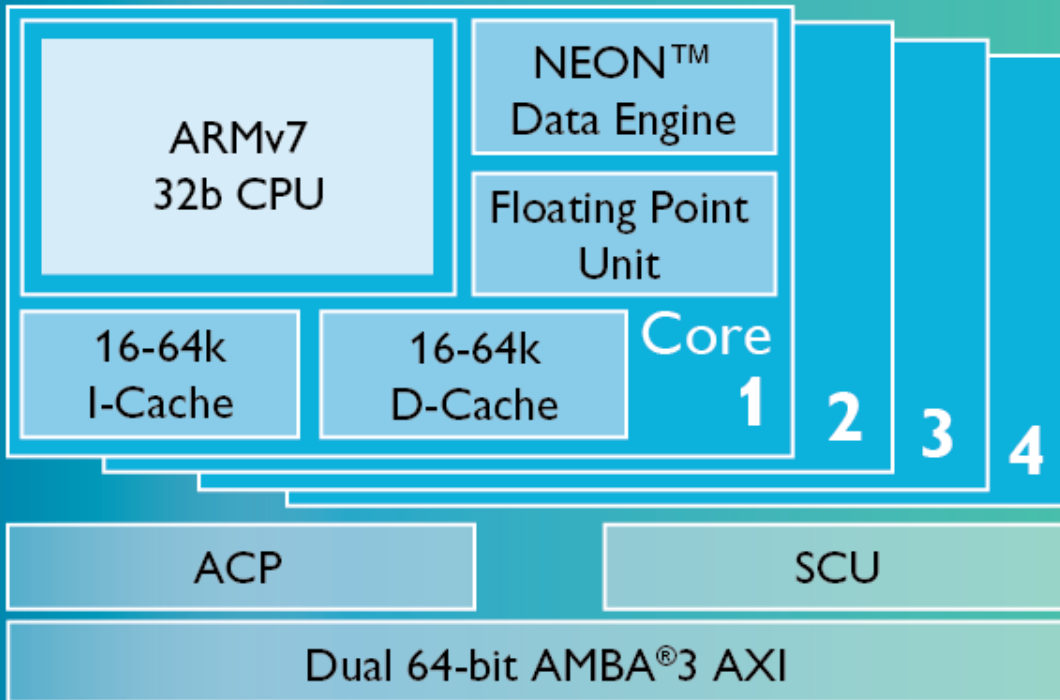
Integrated L2 Cache

64- or 128-bit AMBA<sup>®</sup>3 Bus Interface

AMBA: Advanced Microcontroller Bus Architecture

# ARM<sup>®</sup> Cortex<sup>®</sup>-A9

ARM CoreSight<sup>™</sup> Multicore Debug and Trace



ACP: Accelerator Coherency Port; SCU: Snoop Control Unit

# ARM Cortex-M

Scalable and Compatible Architecture

ARM CORTEX  
Processor Technology  
Cortex-M0



Lowest cost  
Low area

ARM CORTEX  
Processor Technology  
Cortex-M0+



Lowest power  
Outstanding energy  
efficiency

ARM CORTEX  
Processor Technology  
Cortex-M3



Performance efficiency  
Feature rich connectivity

ARM CORTEX  
Processor Technology  
Cortex-M4



Digital Signal Control (DSC)  
Processor with DSP  
Accelerated SIMD  
Floating point (FP)

ARM CORTEX  
Processor Technology  
Cortex-M7



Maximum DSC Performance  
Flexible Memory System  
Cache, TCM, AXI, ECC  
Double & Single Precision FP

Digital Signal Control application space

'8/16-bit' Traditional application space

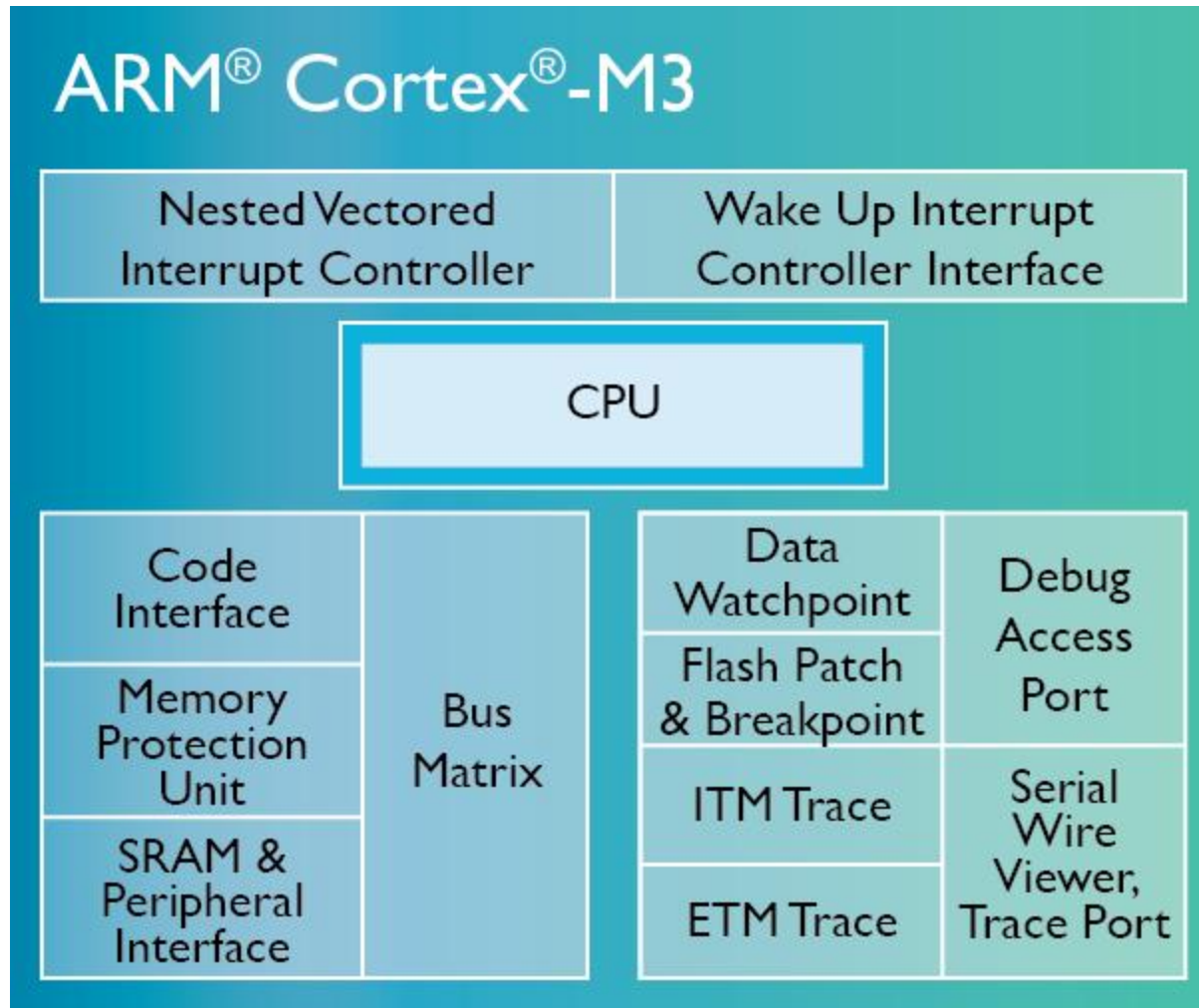
'16/32-bit' Traditional application space

# ARM Cortex-M

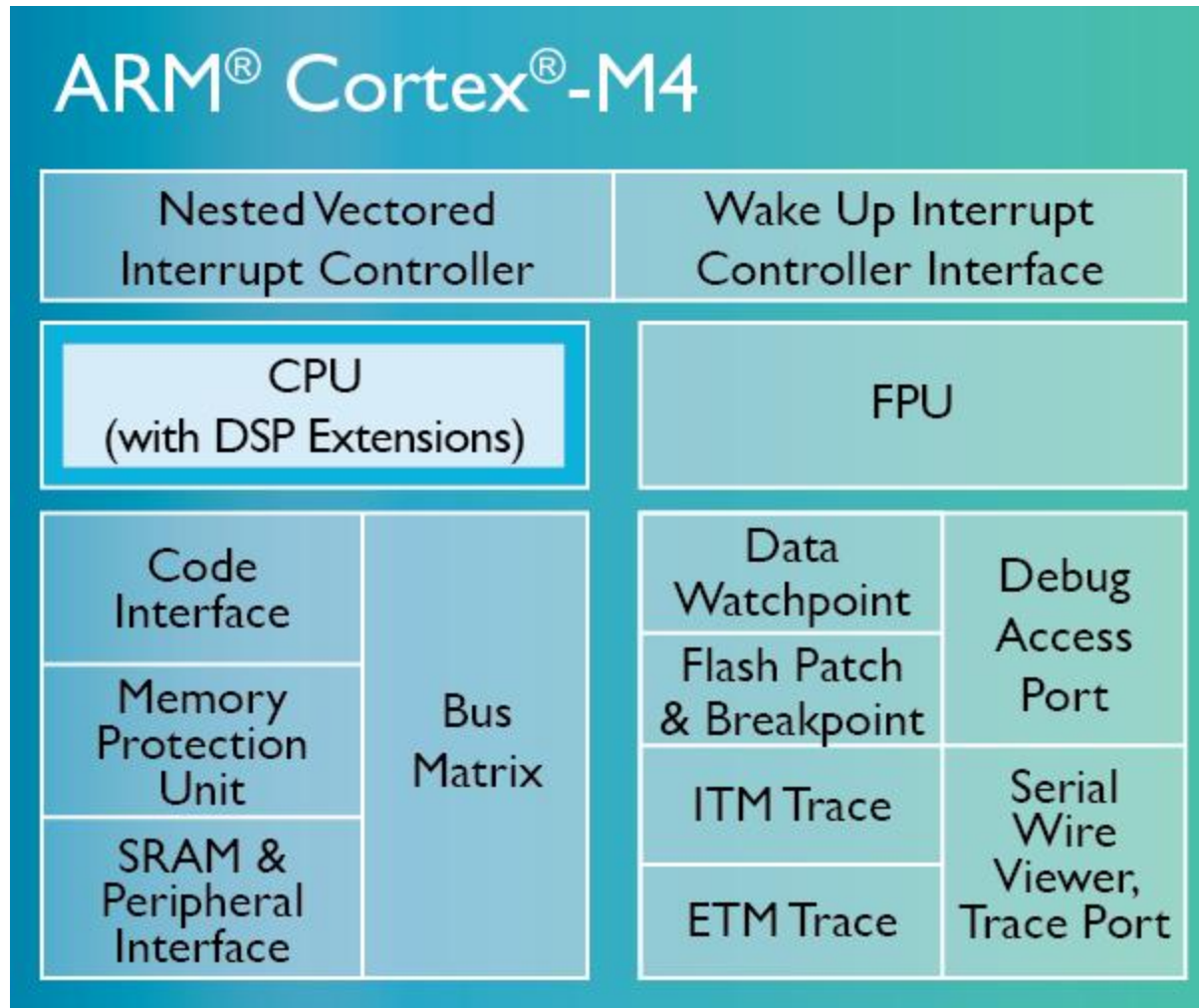
Cortex-M0	Cortex-M0+	Cortex-M3	Cortex-M4	Cortex-M7
Touchscreen controller	IoT sensor node	Activity trackers and basic wearables	Smart metering and sensor fusion	High-end audio headset or soundbar
Power management	Bluetooth smart transceiver	Wifi transceiver	High-performance motor control	Automotive (transmission, body electronics, low-cost infotainment)



# ARM Cortex-M3 Processor



# ARM Cortex-M4 Processor



# ARM Cortex-M4 Processor

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Energy efficient digital signal control

- The Cortex-M4 processor has been designed with a large variety of highly efficient signal processing features
- The Cortex-M4 processor features extended single-cycle multiply accumulate (MAC) instructions, optimized SIMD arithmetic, saturating arithmetic instructions and an optional single precision Floating Point Unit (FPU).

# ARM Cortex-M4 Processor

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## Responsiveness and low power

- The Cortex-M4 has integrated sleep modes and optional state retention capabilities which enable high performance at a low level of power consumption.
- The processor executes the Thumb-2 instruction set for optimal performance and code size.
- The Cortex-M4 Nested Vectored Interrupt Controller is highly configurable at design time to deliver up to 240 system interrupts with individual priorities, dynamic reprioritization and integrated system clock.

# ARM Cortex-M4 Features

<b>ISA Support</b>	<a href="#">Thumb / Thumb-2</a>
<b>DSP Extensions</b>	Single cycle 16/32-bit MAC Single cycle dual 16-bit MAC 8/16-bit SIMD arithmetic Hardware Divide (2-12 Cycles)
<b>Floating Point Unit</b>	Single precision floating point unit IEEE 754 compliant
<b>Pipeline</b>	3-stage + branch speculation
<b>Performance Efficiency</b>	Without FPU: 1.25 / 1.52 / 1.91 DMIPS/MHz* With FPU: 1.27 / 1.55 / 1.95 DMIPS/MHz*

\* Dhrystone **MIPS** (Million Instructions per Second), or **DMIPS**, is a measure of computer performance relative to the performance of the DEC VAX 11/780 minicomputer of the 1970s.

# ARM Cortex-M4 Features

<b>Memory Protection</b>	Optional 8 region MPU with sub regions and background region
<b>Interrupts</b>	Non-maskable Interrupt (NMI) + 1 to 240 physical interrupts
<b>Interrupt Priority Levels</b>	8 to 256 priority levels
<b>Wake-up Interrupt Controller</b>	Up to 240 Wake-up Interrupts
<b>Sleep Modes</b>	Integrated WFI and WFE Instructions and Sleep On Exit capability. Sleep & Deep Sleep Signals. Optional Retention Mode with ARM Power Management Kit
<b>Bit Manipulation</b>	Integrated Instructions & Bit Banding
<b>Debug</b>	Optional JTAG & Serial-Wire Debug Ports. Up to 8 Breakpoints and 4 Watchpoints.
<b>Trace</b>	Optional Instruction Trace (ETM), Data Trace (DWT), and Instrumentation Trace (ITM)