ELC 4384 – RF/Microwave Circuits II Software Project 1: Lumped Element Matching Circuit Design and Analysis Due Thursday, February 6, 2020

Note: This procedure has been adapted from a procedure written by Dr. Tom Weller at the University of South Florida for the RF/Microwave Circuits II course.

In this software assignment, you will follow Example 2.4.2 from the Gonzalez text [1]. In this example, a series L-shunt C configuration is used to transform a load impedance of $(10 + j10) \Omega$ into an input impedance of 50 Ω . You will perform simulations for this matching network and then design a second matching network to transform a load impedance of $(20 + jX) \Omega$ into a 50- Ω input impedance, where X will be a value assigned to you by the instructor (X = 5, 10, 15, 18, 20, -5, -10, -15, or -20)

You will then design matching networks for the same two load impedances in a series C - shunt L configuration and analyze with ADS.

Part 1: Series L-Shunt C Configuration (Gonzalez text Fig. 2.4.8a)

1. Use the $(10 + j10) \Omega$ load for the following steps:

- a) Generate a 1-port schematic containing only a series R-L circuit representing this load impedance.
 - i) Double click on the S-parameter control block in your schematic. Click on the Parameters tab, and check the Z-parameters box. This will allow the calculation of Z parameters. Note that for a one-port network, $Z_{in} = Z_{11}$.
 - ii) Plot the real and imaginary parts of the input impedance to the load on a single rectangular graph, with the real part on the left y axis and the imaginary part on the right y axis, from 0.1 to 1000 MHz. To move the imaginary part to the right y axis, first add the real and imaginary parts of Z₁₁ to a rectangular plot. Double click the plot to open the Plot Traces & Attributes window as shown below in Figure 1. Highlight the imaginary trace under the Traces section and click the Trace Options button. In the Trace Options menu, select the Right Y Axis option in the drop down box and click OK as shown below in Figure 2. Adjust the scale of each axis if needed.

Min Plot Traces & Attributes	<u> </u>	
Plot Type Plot Options	⊕ ▦	
Datasets and Equations	7	Traces
untitled1 -	•	Trace Options
Search	List 🗸	imag(Z(1,1))
freq PortZ PortZ(1)	>>Add >>	real(Z(1,1))
S S(1,1) Z	>>Add Vs>>	
2(1,1)		
	Manage	
Enter any Equation	>> Add >>	
ОК	Cancel	Help

Figure 1. Plot Traces & Attributes Window

Trace Optio	ns:0			×
Trace Type	Trace Options	Plot Axes	Trace Expression	
X avis:		Yavi	5.	
X Axis		▼ Y Ax	is	-
		Y Ax Righ	is t Y Axis	
ОК		Cancel		Help

Figure 2. Trace Options Window

- b) Create a new circuit schematic and add the matching network.
 - Plot the real and imaginary parts of the input impedance on a single rectangular graph, with the real part on the left y axis and the imaginary part on the right y axis, from 0.1 to 1000 MHz.
 - Plot S₁₁ on a single rectangular chart, with dB magnitude on the left y axis and phase on the right y axis.
 - iii) Plot the fraction of the power absorbed in the circuit. The fractional power is given by the equation

$$FractionalPower = 1 - |S_{11}|^2$$

To create this plot, add a rectangular graph to the display window. In the Plot Traces & Attributes window, add the equation **1-abs(S11)**2** to the equation box shown below in Figure 3 and click OK.

ſ	Plot Traces & Attributes
	Plot Type Plot Options
	Datasets and Equations Traces
	Part_1_MatchingNetwork Trace Options
	Freq >>Add >>
	PortZ(1) S ()>>Add Vs>> () () () () () () () () () () () () ()
	Z(1,1)
	Variable Info
Insert equation	Manage
Here	Enter any Equation >> Add >>
l	OK Cancel Help

Figure 3: Plot Traces & Attributes window

2. Repeat steps (a) and (b) above using the $(20 + jX) \Omega$ load. You will need to design the matching network for this load.

Part 2: Series C – Shunt L Configuration (Gonzalez text Fig. 2.4.9a)

Repeat steps 1 and 2 from Part 1 using a series C as the component closest to the load for your matching network designs. You may omit the plots of the load impedances (step (a)), as you have already plotted them in Part 1.

<u>Report</u>

Your report should have a cover sheet with your name on it, the name of the course, and the date of submission. Simulation schematics and data plots should be presented following the order of this procedure with the appropriate steps annotated near the plots and each plot appropriately titled. At the conclusion of the data presentation, answer the following question.

 Give the 3-dB bandwidth (in percent using the design frequency as the "center") for each of the four circuits simulated in this experiment. Calculate the bandwidth from the "power absorbed" plots.
 NOTE: For some matching impedance combinations, your passband may not appear to have a cutoff on one side. In this case, you can simulate out further in frequency to try to find a cutoff. If no cutoff exists, then the 3-dB bandwidth is infinite.

References

[1] G. Gonzalez, *Microwave Transistor Amplifiers: Analysis and Design*, 2nd ed. Prentice Hall, 1996.