ELC 5338 High Frequency Electronics I
Laboratory 9: Stepped-Impedance Low-Pass Filter

Note: This lab procedure has been adapted from a procedure written by Dr. Larry Dunleavy and Dr. Tom Weller at the University of South Florida for the WAMI Laboratory. It has been modified for use at Baylor University by Dr. Charles Baylis.

Printed Name:_____

Lab Partner: _____

Please read the reminder on general policies and sign the statement below. Attach this page to your Post-Laboratory report.

General Policies for Completing Laboratory Assignments:

For each laboratory assignment you will also have to complete a Post-Laboratory report. For this report, you are strongly encouraged to collaborate with classmates and discuss the results, but the descriptions and conclusions must be completed individually. You will be graded primarily on the quality of the technical content, not the quantity or style of presentation. Your reports should be neat, accurate and concise (the Summary portion must be less than one page). Laboratory reports are due the week following the laboratory experiment, unless notified otherwise, and should be turned in at the start of the laboratory period. See the syllabus and/or in-class instructions for additional instructions regarding the report format.

This laboratory report represents my own work, completed according to the guidelines described above. I have not improperly used previous semester laboratory reports, or cheated in any other way.

Signed: _____

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Laboratory Assignment:

Overview

In this laboratory, you will design a distributed-element low-pass filter using the stepped-impedance approach. The filter will have an 0.5 dB ripple, Chebyshev response. The laboratory is split into two sessions. In the first session, you will design, simulate, and generate a layout for your filter. In the second session, you will fabricate and measure your filter, and you will compare your measured S-parameter data with the simulation results.

Laboratory Procedure

Session 1: Design and Simulation

A. Design

1. You will be assigned a cutoff frequency: 1.2 GHz, 1.25 GHz, 1.3 GHz, 1.35 GHz, 1.4 GHz, 1.45 GHz, 1.5 GHz, 1.55 GHz, 1.6 GHz, 1.65 GHz, 1.7 GHz, 1.75 GHz, or 1.8 GHz. Enter your assigned cutoff frequency below:

Cutoff Frequency = _____ GHz

2. Choose the high and low impedance values that you will use for your design as 110 Ω and 20 Ω, respectively. Using your design frequency and the high and low impedance values you will use, design a three-element 0.5 dB ripple, Chebyshev low-pass filter, where the first transmission line is a high impedance line. Sketch your design below, specifying the electrical length and characteristic impedance of each line segment:

B. Linecalc

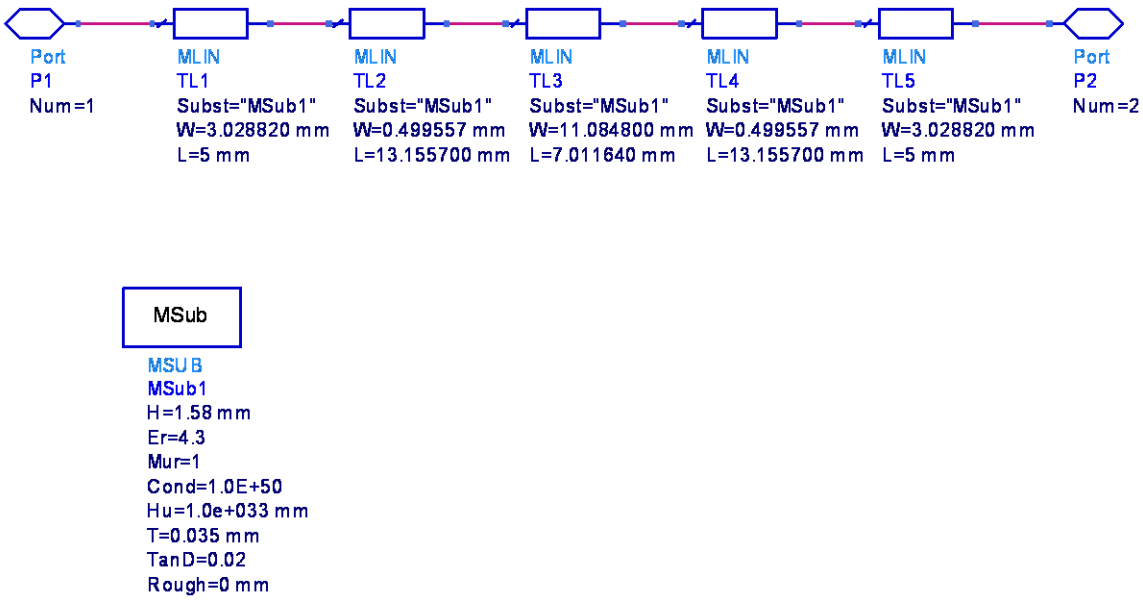
1. Use the Linecalc program in ADS to obtain physical dimensions for your filter sections. Also check the width of the 50 Ω lines you will use at the input and output of your filter. Use the following substrate parameters: h = 1.58 mm, t = 0.035 mm, tand = 0.02, and ϵ_r = 4.3. Make sure that you perform the calculations using your assigned cutoff frequency. Record the results in the following table:

Cutoff Frequency (GHz)	
50 Ω Line Width (mm)	
Sections 1 and 3:	
Prototype Element Value	
Characteristic Impedance (Ω)	
Electrical Length (Degrees)	
Width (mm)	
Length (mm)	
Section 2:	
Prototype Element Value	
Characteristic Impedance (Ω)	
Electrical Length (Degrees)	
Width (mm)	
Length (mm)	

C. ADS Simulations

Note: When you create the circuit schematics in the following steps, position each of the elements you use in an orderly fashion, starting with Port 1 on the left and ending with Port 2 on the right. This approach will help in avoiding problems when you use the automatic layout generation feature.

1. Generate an ADS circuit schematic that represents your lowpass filter, using MLIN elements as appropriate, with an MSUB block giving the same substrate parameters as the ones you used in the above section. This will be a two-port network that consists of the following: (a) microstrip line element representing a 5 mm long, 50 Ω input line, (b) three sections of microstrip lines representing your filter sections, and (c) 5 mm long, 50 Ω output line. Note: Do not use MSTEP elements yet; we will use these in a later step to investigate the effect of modeling the discontinuities in the line segments. Your filter schematic should look similar to the one below. Save the design as lpfd1.dsn.



2. Obtain a copy of this schematic for your report.

3. Now you will create an additional circuit schematic that will provide a more accurate prediction of the filter response. Add appropriate MSTEP elements between the MLIN sections to account for the step discontinuities. As discussed in previous laboratory exercises, this models the fringing effects that occur when a wide line connects to a narrower line and vice versa. It also accounts for the associated change in the effective length of each line. Save this design as lpfd2.dsn.

4. Obtain a copy of the lpfd2.dsn schematic for your report.

5. Construct a higher level schematic, titled lpfd_lab.dsn, and create references to the lpfd1.dsn and lpfd2.dsn schematics. Insert an S-parameter simulation control block that enables S-parameter simulation from 300 kHz to 6 GHz with 401 data points. Compare the responses between the lpfd1 and lpfd2 designs. You should notice a slight difference in the frequency response of the two circuits.

D. Layout Generation

ADS has a feature that allows automatic generation of a layout from a circuit schematic. In a previous laboratory exercise, you manually generated a layout using polylines. In this experiment, you will automatically generate the layout.

1. In the circuit schematic window, open the lpfd2.dsn schematic.

2. Pull down the Layout menu at the top of the schematic window and select Generate/Update Layout. At this point a Generate/Update Layout pop-up window will appear. This window allows you to re-position some of the elements if required. Click OK. Then click OK in the Status of Layout Generation pop-up window. You will now find that a layout corresponding to your circuit schematic has been created.

3. Delete the ports (shown by arrows) from the layout.

4. Go to Options → Layers. Click on the None Visible button and then click on Apply. Select Cond in the list of layers, click on the Visible box and then Apply. In the Shape Display list, select Outline and then click Apply. Click OK to close the layer editor window.

5. The next step is to set the size of the connecting pins to zero. Go to the Options pull-down menu and select Preferences. Click on the Pin/Tee tab at the top of the pop-up window, and enter a size of 0 for both pins and tees. Click on Apply and then OK.

6. Click on Options → Preferences and select the Units/Scale tab. Check the scale factor for Length in mm, click on Apply and then OK.

7. Click on File → Export and select the DXF file type, enter the filename, and click on "OK".

8. Save copies of the .dxf version and the circuit design file, lpfd2.dsn, and turn them in at the end of the first session.

Session 2: Measurement

1. Assemble your filter by attaching an SMA connector at each of the ports. The connectors should fit snugly, and you will not use solder since the connectors will need to be reused for other laboratory experiments.

2. Calibrate the VNA to measure from 300 kHz to 3 GHz, using 401 data points. Take a two-port S-parameter measurement of your filter design and save the data as a .s2p file.

3. Generate a circuit schematic in ADS that represents your measured data file, and name the design something such as dislpf_dat.dsn. Recall that you can obtain a two-port S-parameter data box from the Data Items palette.

4. Open the higher-level schematic (lpfd_lab). Add a reference to the dislpf_dat.dsn schematic to allow viewing of the measured data.

5. Perform the simulation and generate one plot that contains both S11 and S21 in dB for the measured results and the lpfd1 and lpfd2 simulation results for the entire measured frequency band (hopefully 300 kHz to 3 GHz). Obtain a copy of this comparison plot for your report.

Report

Your report should contain the following:

1. A brief description of the laboratory assignment (Summary)

2. The filter parameter table showing the line dimensions obtained using Linecalc

3. The copy of the ADS filter circuit schematics, with and without the MSTEP elements

4. The plot comparing predicted (simulation) performance with and without the MSTEP elements

5. The plot from ADS that compares the measured results to the results of the ADS circuit model simulations

6. A brief, well-written discussion of results discussing the following:

   A. What is the maximum out-of-band attenuation of your filter that you were able to measure?

   B. At approximately what frequency did your design stop acting as a "lowpass" filter.

   C. What effect did including the MSTEP elements have on the predicted filter response? What does this say about the "effective" electrical length of the filter sections? (Note: If the measured and predicted filter responses differ, part of the error could be caused by the range of validity for the MSTEP element in the ADS models. The documentation states that the model for this element is accurate for ratios of W2/W1 between 0.1 and 10.)

   D. Why does the performance of this type of filter deviate from the "ideal" lowpass filter response (e.g. one using perfect capacitors and inductors) as the frequency increases?