ELC 4383 RF/Microwave Circuits I
Laboratory 4: Quarter-Wave Impedance Matching Network

Note: This lab procedure has been adapted from a procedure written by Dr. Larry Dunleavy and Dr. Tom Weller at the University of South Florida for the WAMI program and from related procedures written for the WAMI Laboratory. It has been modified for use at Baylor University by Dr. Charles Baylis.

Printed Name:_____

Please read the reminder on general policies and sign the statement below. Attach this page to your Post-Laboratory report.

General Policies for Completing Laboratory Assignments:

For each laboratory assignment you will also have to complete a Post-Laboratory report. For this report, you are strongly encouraged to collaborate with classmates and discuss the results, but the descriptions and conclusions must be completed individually. You will be graded primarily on the quality of the technical content, not the quantity or style of presentation. Your reports should be neat, accurate and concise (the Summary portion must be less than one page). Laboratory reports are due the week following the laboratory experiment, unless notified otherwise, and should be turned in at the start of the laboratory period. See the syllabus and/or in-class instructions for additional instructions regarding the report format.

This laboratory report represents my own work, completed according to the guidelines described above. I have not improperly used previous semester laboratory reports, or cheated in any other way.

Signed: _____

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Laboratory Assignment:

Overview

This laboratory exercise involves the design and measurement of a 2 GHz quarter-wave impedance matching network. In the first part of the exercise, you will design a quarter-wave matching network to match given resistor to a 50 ohm transmission line using Linecalc, a tool available in Advanced Design System (ADS) for performing calculations related to transmission lines. You will then simulate your design in ADS. Finally, your design will then be fabricated in the laboratory and in the second session, you will measure the input reflection coefficient of your network. You will then have an opportunity to compare simulation and measurement results and make some observations regarding non-ideal effects that manifest themselves in measurement data.

NOTE: Any section displayed as [OPTIONAL] is optional for any students taking the course for undergraduate credit but is required for students taking the course for graduate credit. Students taking the course for undergraduate credit that complete these sections can receive up to 1 extra-credit point (out of 10) on this laboratory assignment (maximum score 11 out of 10).

Procedure

Session 1:

A. Initial Calculations

Note: Your design frequency for the match is 2 GHz.

1. You will be assigned a load resistor value. Write the value of this resistance here: _____Ω

2. Calculate the characteristic impedance of a quarter-wave matching network section to match this impedance to a 50-ohm system:

Quarter-Wave Matching Network Characteristic Impedance: _____Ω

Create a workspace and select "Standard ADS Layers, 0.0001 millimeter layout resolution" from the "Technology" window.

B. Linecalc

Linecalc is a feature in ADS that can be used to calculate characteristic impedance and electrical length given length and width of a transmission line on a given substrate, or vice versa.

1. After opening a schematic window in ADS, go to Tools → Linecalc → Start Linecalc. A new window will open up in the screen.

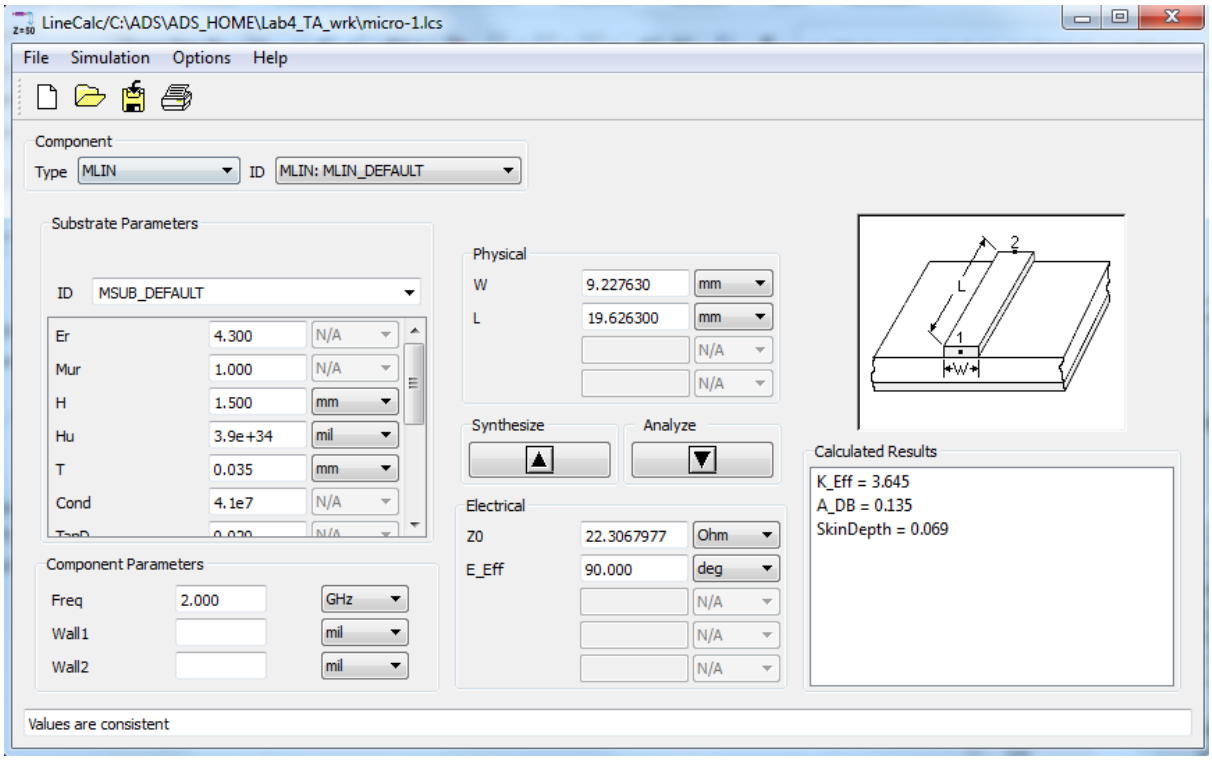

Figure 1: ADS LineCalc Window

2. Go to File → Save As, and enter micro-l.lcs as the name of the file.

There are four "areas" in the Linecalc window. The top left area allows you to enter parameters of the substrate you will be using (such as relative permittivity, loss tangent, and substrate thickness). The bottom left area allows you to enter the frequency. On the right hand side of the screen you will see two arrows: one is labeled "Synthesize" and the other is labeled "Analyze". If "Synthesize" is chosen, then the width and length of the line are calculated based on the user entries for characteristic impedance and electrical length. If "Analyze" is selected, then the characteristic impedance and electrical length of the line are calculated based on the physical width and length.

3. Enter the frequency as 2.0 GHz.

4. Enter the substrate parameters as follows:

h	1.50 mm
t	0.035 mm
ε_r	4.3
tand	0.02

Table 1: M-Sub Substrate Values

h = 1.50 mm (substrate thickness), t = 0.035 (metal thickness), ε_r = 4.3 (relative permittivity), tand = 0.02 (loss tangent). Enter the electrical length, E_eff = 90 degrees, because a quarter-wavelength transmission line has an electrical length of 90 degrees. Before clicking the synthesize button, make sure the width and length parameters have the units of millimeters.

5. Synthesize to find the geometry of the quarter-wavelength line.

f_c (GHz)	50 Ω Line Width (mm)	Width in Matching Section (mm)	Length in Matching Section (mm)	Width in RF Short Section (mm)	Length in RF Short Section (mm)

6. You will use another quarter-wavelength transmission line terminated in an open circuit to "connect" the load to RF ground. This is possible because, at the frequency at which this line is a quarter wavelength long, the open circuit at the end of the transmission line is transformed to appear as a short circuit. One reason for using an "RF short" is to avoid the need to drill through the board to form a via-hole connection to the physical ground plane on the back side of the microstrip. Use Linecalc to calculate the width in the RF short section and its length (a quarter-wavelength). You may choose any characteristic impedance that is less than or equal to 50 Ω, but the line width should not be greater than 10 mm. Write the results in the last two columns of the above table.

7. Find the width of a 50 Ω line using the synthesis key. Enter this line width in the above table.

8. Make a pencil-and-paper sketch of your circuit's layout. You should have a 10 mm, 50 ohm line, followed by the quarter wave matching section, followed by a 1 mm gap (for the resistor), followed by the RF short.

C. Simulations

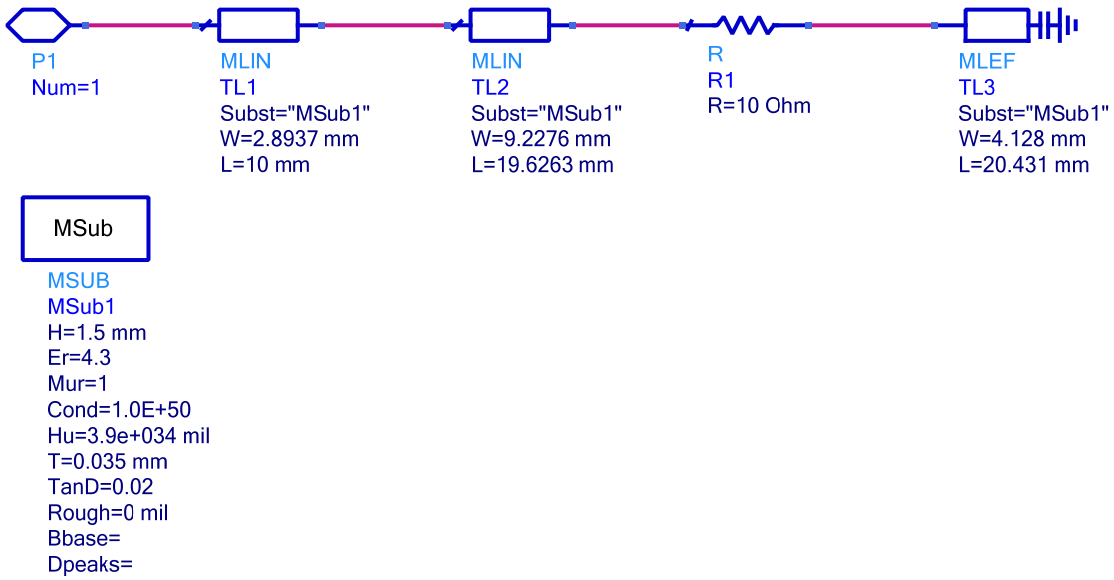

Figure 2: Matching network schematic

1. Open a new schematic window in ADS. Create the circuit shown in figure 2 with the width and length values calculated in section B. Go to File → Save As, and name your schematic cell lastname_4, where you insert your last name.

2. Select the Tlines-Microstrip palette and place an MSUB component in the schematic. Use the same settings you used for your Linecalc simulations in the previous section.

3. Add a microstrip transmission line element. Select an MLIN element from the Tlines-Microstrip palette and place it into the design. Use it to represent the 10 mm, 50 Ω input line. Use the width calculated by Linecalc.

4. Add a second MLIN element to represent the quarter-wave matching section. Use the length and width calculated by Linecalc above.

5. Go to the Lumped Components palette and select a resistor. Place a resistor with **your** design value into the schematic.

6. Add the RF short to the schematic. Reselect the Tlines-Microstrip palette and select MLEF (Microstrip Line Open-End Effect). We will use this component instead of MLIN because it calculates effects due to fringing electric fields on the end of the transmission line. These fringing fields will increase the effective electrical length of the line.

7. Attach a port to the 10 mm, 50 ohm line to allow reference from a higher-level schematic. The completed schematic look similar to the schematic shown in Figure 2, with your design values in place rather than the ones shown.

Save your design. Place a copy of your schematic in your report.

8. Change your resistor value to 200 Ω and rename the schematic cell as matcktb. Calculate the required characteristic impedance of the quarter-wave transformer to match 200 Ω to a 50 Ω system, and use Linecalc to calculate the dimensions of the new matching section. Adjust your schematic accordingly.

9. [OPTIONAL] Create a third design, rename the schematic cell matcktc. Repeat the above procedure for a load of 75 Ω.

10. Create a higher-level schematic and rename the schematic cell matckt_lab that references matckt, matcktb, and (if applicable) matcktc.

11. Set up an S-parameter simulation to simulate from 300 kHz to 5 GHz. Plot $|S_{11}|$ (Transmission) in dB for all three of the matching networks. At this point, you should see a minimum in $|S_{11}|$ at 2 GHz (your design frequency) for each matching circuit. Obtain a copy of the plot for your report. Examine the difference in bandwidth of the three matching circuits by finding which matching circuit provides the lowest value of S_{11} over the largest frequency range.

12. [OPTIONAL] Examine the result caused by a complex load impedance. Open lastname_4 and rename the schematic cell as matcktd. Delete the load resistor. Go to the Lumped-Components palette and place a SRL (Series Resistor-Inductor) into the schematic. Specify the value of the resistance as your design value and the inductance as 10 nH. Place the SRL between the matching section and the RF short in your schematic.

13. [OPTIONAL] Click File, Save As and rename schematic cell matcktd to matckte. We will attempt to add a capacitance to cancel the load inductance at the 2 GHz design frequency (keep in mind that this cancellation can occur at precisely one frequency). Calculate the value of capacitance that will combine with the 10 nH inductance in series to produce a net reactance of zero at the 2 GHz design frequency. Place a capacitor with this value between the SRL component and the quarter-wave impedance transformer.

Value of Capacitor to "Cancel" Inductive Reactance at 2 GHz = _____ pF

14. [OPTIONAL] Add references to matcktd and matckte from matckt_lab. Simulate S_{11} for the lastname_4, matcktd, and matckte networks and plot the results from 300 kHz to 5 GHz. Obtain a labeled copy of the plot for your report.

How do these matching circuits perform differently?

Why?

D. Layout

You will use ADS to generate a layout of your matching circuit for fabrication.

1. Open the lastname_4 schematic. Go to the Layout tab and click "Generate/Update Layout". Click OK in the dialog box that opens.
2. Delete the parts P1 and R1 from your layout.
3. Make sure that the components are connected and there is a 1 mm gap between the RF short and matching section.
4. Now, create the outline of your board by first clicking on the drop down box labeled v,s default:drawing. Click the "Insert Rectangle" button and draw a rectangle around the matching circuit in the Layout window. Be sure that the transmission line at the input of the matching network (on the left of the circuit) is at the edge of the board, as shown below in Figure 6. The rectangle needs to be at least 10 mm wide.
5. Save your layout.

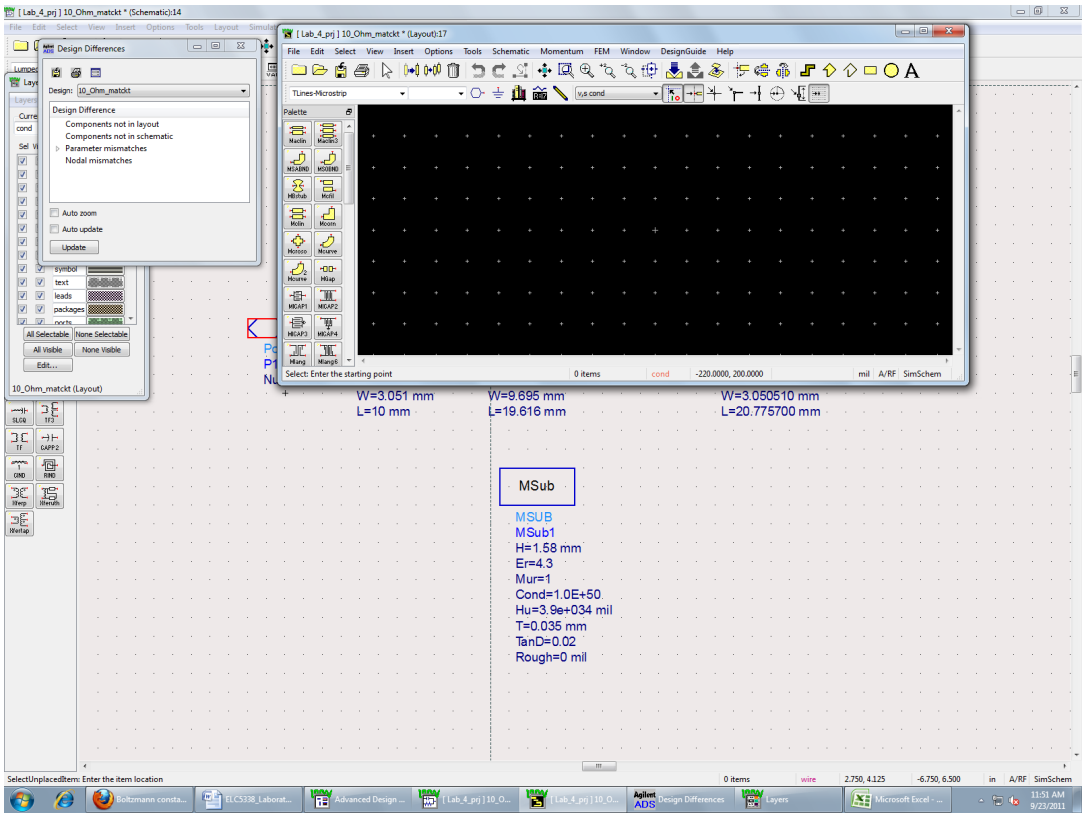

Figure 4: ADS Schematic view with layout window.

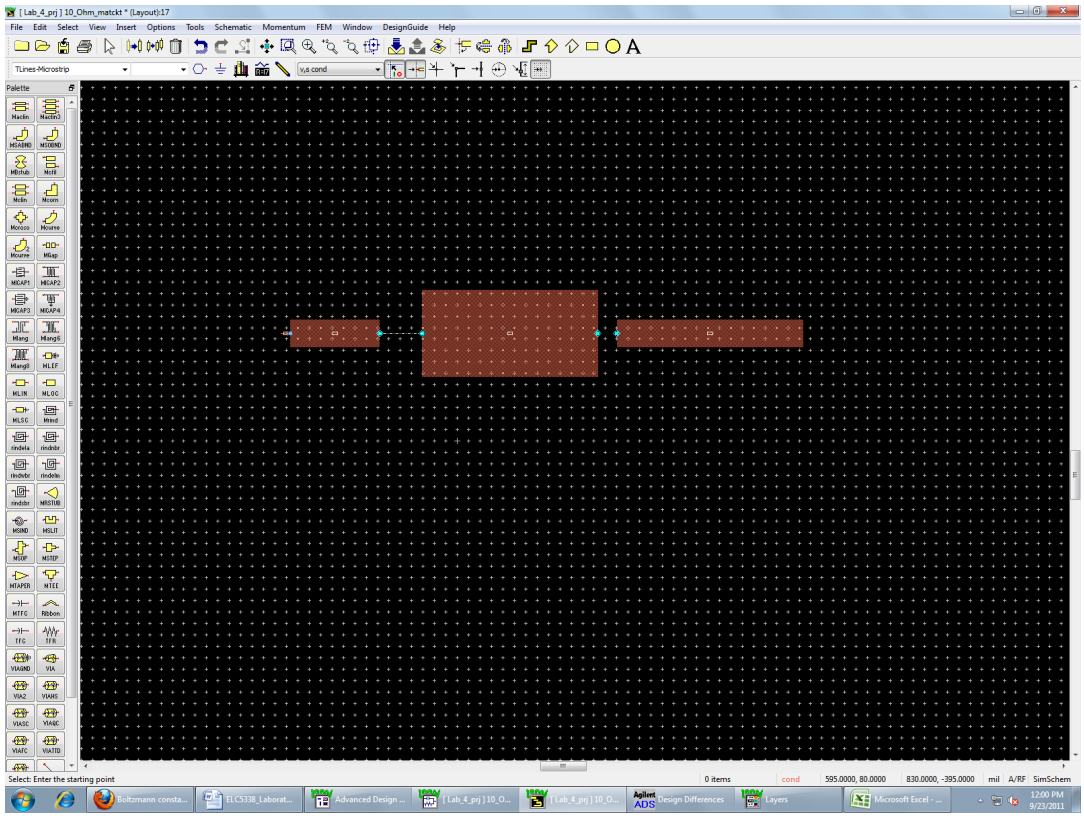

Figure 5: Design layout window

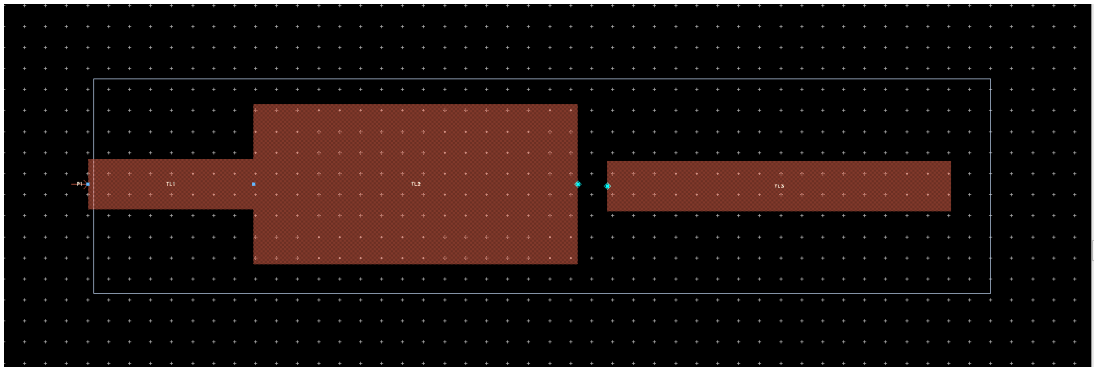

Figure 6: Layout with board outline

8. Export the file by going to File → Export and select "Gerber" as the file type. Check the box for "View file after export". Click More Options and change the Fractional digits to 6. Under the Layers tab, make sure the export check box is checked for default and cond. Press OK and ignore and close the error/warning window that comes up.

Provide two files to the teaching assistant: the Gerber file and the lastname_4 schematic file (your layout in ADS form). Both of these files should be named using the naming convention given above.

Session 2:

In Session 2 you will measure the input reflection coefficient of your design over frequency using a VNA and compare the measured data to simulation results.

A. Assembly and Measurement of Circuit

1. Assemble your matching circuit. First, solder the resistor between the quarter-wave transformer and the RF short (over the 1 mm gap from the layout). Attach an SMA connector to the board edge in order to contact the 50 Ω line. Do not use solder; you will need to re-use the connector in future lab experiments. Use a multimeter to verify the resistance of the chip resistor.

2. Calibrate the VNA from its low-frequency limit to 3 GHz. Connect a coaxial cable to port 1 of the VNA. Perform a Reflection Calibration on port 1 of the VNA. Be sure to enter the calibration standard definitions for the calibration kit.

3. Connect your matching circuit to the coaxial cable. If your design is correct, expect to see a reflection coefficient minimum at or near 2.0 GHz, your design frequency.

4. Save the data as a .s1p file for viewing using ADS on a thumb drive.

B. Comparison of Simulation and Measurement Data Using ADS

1. Using ADS, generate an .s1p data box to represent your measured data. Attach a ground to the REF port of the box on the right side and a port to the left side. Save the schematic cell as matdat.

2. Now open the higher-level schematic generated in Session 1, matckt_lab, and add a reference to the matdat schematic. Perform a simulation and generate a plot that contains S_{11} (dB) for the model of the matching circuit design and the measured results. The plot should cover the entire range of frequencies for which the measurement was performed. Be careful not to use frequency points outside the range of the measured data as ADS will erroneously extrapolate the measurement data. Include this plot in your report.

Report

For your report, include the following:

1. The usual Summary of up to one-half page in length

2. A copy of your hand-sketched circuit layout

3. Your ADS matching circuit schematic

4. Simulation comparison plots comparing results from lastname_4, matcktd, and matckte

5. The plot from ADS comparing the measured and simulation (lastname_4) results.

6. Discussion of Results: Answer the following questions with a brief but well-written discussion:

   A. How are the measured and simulated input reflection coefficient plots of your matching circuit different?
   B. Give some possible reasons for these differences. (Hint: recall Lab 3 on passive component modeling. Also consider the effects that fringing fields will have on the effective length of the transmission lines).
   C. In the simulation comparison of the three matching circuits with different load impedances (lastname_4, matcktb, and if applicable, matcktc), which one gave the lowest reflection over the widest bandwidth? For each circuit, calculate the percent bandwidth, $(f_{high} - f_{low})/f_c$ x 100%, over which the reflection coefficient is less than -20 dB. What can you conclude from this experiment?
   D. [OPTIONAL] Recall the simulation regarding the complex load. When the capacitor was placed in series to cancel the load inductance (matckte), did the results match those of the purely resistive load (lastname_4) over the entire frequency range? Why or why not?