Course Schedule and Assignments for ELC 3314 – Spring 2020

Date	Day	Lect.	Lecture Topics	Chapter	Pages	Problems
1/14	T	1	Introduction/Preliminaries, Electronic Systems, The Design Process, Integrated Circuits, Basic Amplifier Concepts	1	1-22	1.15, 1.16, 1.17, 1.18
1/16	R	2	Cascaded Amplifiers, Power Supplies and Efficiency, Decibel Notation, Amplifier Models, Ideal Amplifiers, Amplifier Frequency Response, Differential Amplifiers	1	23-53	1.21, 1.27, 1.31, 1.38, 1.42, 1.45, 1.63
1/21	T	3	QUIZ 1, Ideal Operational Amplifier, Summing-Point Constraint, Inverting Amplifier, Noninverting Amplifier	2	61-74	2.10, 2.14, 2.18, 2.25
1/23	R	4	Op-Amp Imperfections in the Linear Range of Operation	2	82-89	2.45
1/28	T	5	QUIZ 2, Large-Signal Operation, DC Imperfections	2	89-100	2.51, 2.58
1/30	R	6	Collection of Amplifier Circuits, Integrators and Differentiators	2	108-121	-
2/4	T	7	QUIZ 3, Diode Characteristics, Load-Line Analysis, Ideal Diode Model	3	132-139	3.10, 3.15, 3.16, 3.17
2/6	R	8	Rectifier Circuits, Wave-Shaping Circuits, Diode Logic Circuits, Voltage-Regulator Circuits	3	139-156	3.20, 3.24
2/11	T	9	QUIZ 4, Linear Small-Signal Equivalent Circuits, Basic Semiconductor Concepts	3	156-169	3.51, 3.56, 3.58
2/13	R	10	Physics of the Junction Diode, Switching and High-Frequency Behavior	3	169-174	3.71, 3.72, 3.87
2/18	T	11	QUIZ 5, Basic Operation of the *npn* Bipolar Junction Transistor, Load-Line Analysis of a Common-Emitter Amplifier, The *pnp* Bipolar Junction Transistor	4	212-231	4.5, 4.10, 4.11, 4.14
2/20	R		TEST 1: Chapters 1, 2, and 3, Closed Book, Closed Notes			
2/25	T	12	Large-Signal DC Circuit Models, Large-Signal DC Analysis of BJT Circuits (Part 1)	4	232-248	4.28, 4.33
2/27	R	13	Large-Signal DC Analysis of BJT Circuits (Part 2)	4	248-368	4.34, 4.38
3/3	T	14	QUIZ 6, Small-Signal Equivalent Circuits, Common-Emitter Amplifier	5	287-334	4.42, 4.45
3/5	R	15	Emitter Follower	5	414-432	4.51, 4.53, 4.60
3/10, 12	T,R		NO CLASS: Spring Break			
3/17	T	16	QUIZ 7, NMOS Transistors, Load-Line Analysis, Bias Circuits, Small-Signal Equivalent Circuits	5	287-313	5.3, 5.6, 5.21, 5.23, 5.24
3/19	R	17	Common-Source Amplifier, Source Follower, JFETs/Depletion-Mode MOSFETs/p-Channel Devices	7	313-334	5.38, 5.40, 5.47
3/24	T	18	QUIZ 8, IC Biasing with BJTs, IC Biasing with FETs	7	414-432	7.15, 7.16, 7.31
3/26	R	19	Large-Signal Analysis of the Emitter-Coupled Differential Pair	7	432-443	7.42
3/31	T	20	QUIZ 9, Small-Signal Equivalent-Circuit Analysis, Design of the Emitter-Coupled Differential Amplifier, Source-Coupled Differential Pair	7	443-465	7.49, 7.58, 7.59
4/2	R		IEEE Texas Symposium on Wireless and Microwave Circuits and Systems	-	-	Summary Assignment
4/7	T	21	Bode Plots, The FET Common-Source Amplifier at High Frequencies, Miller Effect	8	484-510	8.7, 8.8, 8.12, 8.14, 8.20, 8.26
4/9	R		TEST 2, Chapters 4, 5, and 7, Closed Book, Closed Notes, Formula Sheet Provided			
4/14	T	22	QUIZ 10, Hybrid-Pi Model for the BJT, Common-Emitter Amplifiers at High Frequencies,	8	510-523	8.38, 8.40
4/16	R	23	Common-Base, Cascode, and Differential Amplifiers, Emitter Followers, Low-Frequency Response of RC-Coupled Amplifiers Effects of Feedback on Gain, Reduction of Nonlinear Distortion and Noise	8	523-545	
4/21	T		NO CLASS: Diadeloso			
4/23	R	24	QUIZ 11, Input and Output Impedances, Practical Feedback Networks, Design of Feedback Amplifiers, Transient and Frequency Response	9	555-602	9.5, 9.6
4/28	T	25	QUIZ 12, Effects of Feedback on Pole Locations, Gain Margin and Phase Margin	9	602-622	
4/30	R	26	Dominant-Pole Compensation, Oscillator Principles, Wien-Bridge Oscillator, Review for Final Exam	9	622-629 636-647	
5/7	R		FINAL EXAM: Cumulative, 4:30 – 6:30 p.m., Closed Book/Closed Notes, 2 hours			