RF/Microwave Circuits I Laboratory #5

Diode Matching Circuit

Overview

In this laboratory you will design a matching circuit for a simple diode circuit. The design process includes a type of simulation that you have not yet performed: large-signal S-parameter. This is a non-linear simulation that accounts for power level-dependent behavior of the diode.

The design flow is as follows:

- **Part I**: Generate a simplified schematic involving a diode and determine the RF input impedance at various signal input levels (of primary importance is the impedance in the **1.8-2.2 GHz** frequency range).
- **Part II**: Based on the diode input impedance results, design and integrate a two-element lumped matching network (using ideal elements)

Note that you will be simulating with a single, swept frequency power source. It is important to see how the diode behaves at different drive levels and over a band of frequencies near the center frequency.

The basis for the non-linear simulations performed is the "harmonic balance" routine. In the control blocks for these simulations you specify the maximum "order" to be considered, which refers to the highest harmonic number of a given source frequency (e.g. the 3rd harmonic of a signal will be included in the simulation if the order for that source is 3). A consequence of specifying a high order is that all components in the schematic must be valid at the given harmonic frequencies. If, for example, you were using measured data as a "component" in the schematic, and the data file did not extend to the highest frequency used in the harmonic balance analysis, an error would occur. It is also important to consider that many of the component library models available in ADS have a limited range of frequency over which they are valid, and thus some basic inaccuracies in terms of higher-order harmonic results can be expected.

The diode circuit model that you should consider during the experiment is shown in *Figure 1*. You will be asked at some point to determine the effective junction resistance (R_j) and capacitance (C_j) based on simulated S_{11} (or input impedance) data. **The input impedance will be that of the entire diode, but if the series resistance R_s is known, the values for R_j and C_j can be extracted**.

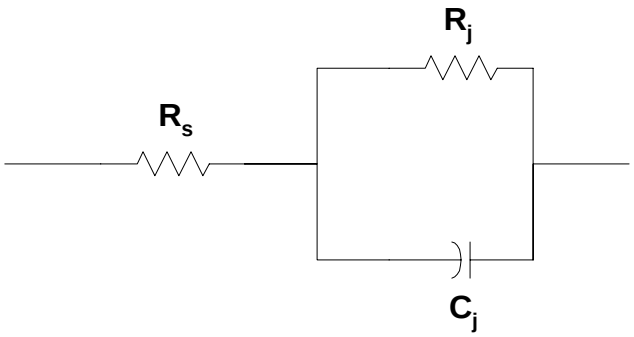

Figure 1. Simplified diode circuit model without package parasitics.

As you complete the experiment you will be asked to fill in various sections with simulation results. For the laboratory report, it is acceptable to submit copies of the relevant pages from this procedure, rather than re-creating the tables, etc.

PART I. Diode and Tuning Stub Schematic

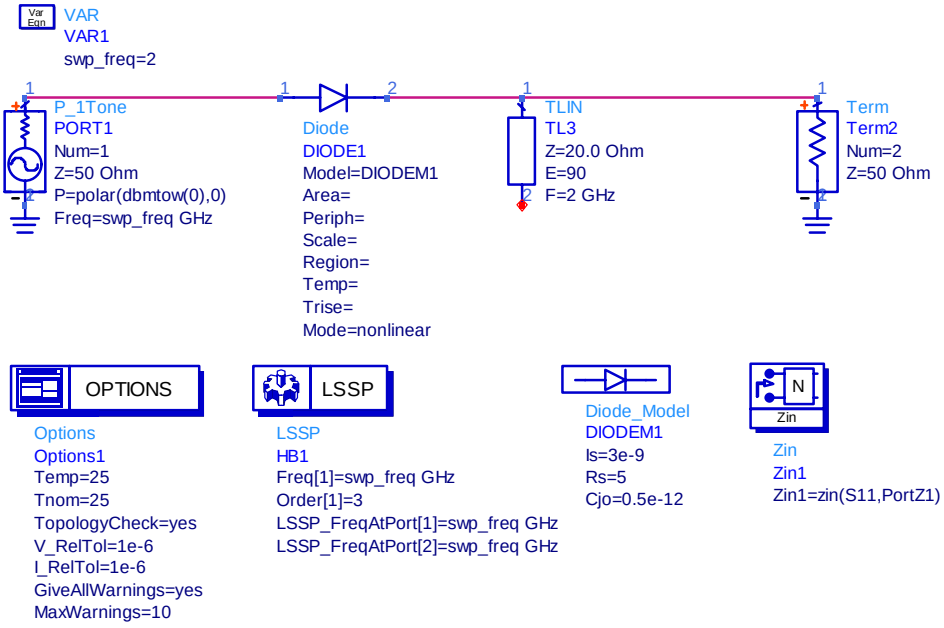

Figure 2. Initial schematic used for large-signal S-parameter simulation of the diode.

1) The first step is to create the schematic that is shown in Figure 2.

a) Select the Tlines-Ideal option from the Component Palette List and place an ideal TLIN element in the schematic. Set the impedance to 20 Ohm, the electrical length to 90 deg and the frequency to 2 GHz. The purpose of this TLIN is to isolate the Port 2 impedance (50 Ohms). The simulator may give a warning because one of the nodes of the TLIN is not connected, but this will not affect the simulation results.

   i) How does this TLIN isolate the port 2 impedance from the rest of the circuit?

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b) Select the Devices-Diodes option from the Component Palette List.

c) Click on the Diode:P-N Junction Diode icon (upper right-hand corner) and place a copy into your schematic.

d) Click on the Diode_Model:P-N Junction Diode Model (DiodeM) icon and place a copy into your schematic. Set the parameter values as shown in the figure, i.e. Is=3e-9 A, Rs=5 Ohm, and Cjo=0.5e-12 F. (Recall the Cjo is the zero-bias junction capacitance.) The remaining parameters should be left at the default values. (You can arrange to have only Is, Rs and Cjo shown on the schematic by "unselecting" the *Display parameter on schematic* option for the others.)

e) Add a Var block to the main (diode) schematic.

   i) Create a variable called swp_freq and assign a value of 2.

   ii) The swp_freq variable will be used to perform swept frequency, large-signal S-parameter simulations, as seen in the proceeding steps. The large-signal simulations differ from the small-signal simulations performed in previous laboratories, in that they are nominally (or, by default) only performed at a single frequency point. In this case, '2' is just a starting value for the frequency sweep – it does not matter what value is specified since it will be over-ridden in later steps in this procedure; what is important is to have *some* variable defined.

f) Select the Simulation-LSSP option from the component palette list.

   i) Add an Options block to the diode schematic. You do not have to change any of the default parameter values.

   ii) Add an LSSP:Large-Signal S-parameter Harmonic Balance Simulation block to the schematic. Double-click on the LSSP block:

      (1) Under the Freq tab, set the Frequency to swp_freq, select the units as GHz and click on Apply.

      (2) Under the Sweep tab, set the *Parameter to sweep* to swp_freq. Set the Start to 1.8, the Stop to 2.2, and the Step-size to 0.05.

(3) Under the Ports tab, set the Port 1 Frequency to swp_freq, select the units as GHz and click on Apply and then Add. Click on Add again, and it will automatically add Port 2 to the list, with the same frequency. (These settings tell ADS the frequencies at which to calculate the S-parameters at the corresponding ports. This is important in a harmonic balance simulation, because in addition to a given swp_freq signal, there will also be harmonics of this signal that are present; in this case, up to 3 harmonics will be included, as specified by the "Order" setting under the Freq tab.)

(4) Under the Solver tab, select the Direct solver option (the Krylov option may be required for your simulations – if you have convergence problems you should try different solvers).

(5) Under the Display tab, you can select the parameters that will be displayed on the schematic.

(6) Under the Params tab, there is a box to set the number of iterations (in the "convergence" area). The harmonic balance simulation is an iterative approach, in which the linear and non-linear portions of the schematic are successively analyzed until the harmonics of the current and voltage and the adjoining terminals are continuous. If, after performing a simulation, a message is returned that the solution did not converge, you may solve the problem by increasing the setting for the maximum iterations. (In developing this procedure, I did not find it necessary to modify the default value of 10.)

iii) Add a zin:port input impedance block to the schematic. This icon can be found in the list on the left-hand side of the schematic window (you may have to scroll down to find it). Notice that this block contains a variable called Zin1. After performing the simulation, you will find this variable among the list of data that can be plotted in the display window.

iv) Add a P_1Tone:Power Source: Single Frequency to the left-hand side of the diode schematic.

(1) Double-click on the P_1Tone and set the Freq variable to swp_freq. (Make sure the units are specified as GHz.)

(2) The **power level for this source** is set by the P variable. You specify a value (in dBm) by changing the number inside the first parentheses (the second number represents the phase). For example, P= polar(dbmtow(5),0) corresponds to 5 dBm at zero degrees phase angle.

(3) For the large-signal S-parameter simulations, it is required that the source port be port 1 (i.e. Num=1 in the parameter list). (This happened by default for us since we placed the P_1Tone in the schematic first among the terminations.)

v) Add a Term to the right-hand side of the diode schematic.

vi) Ground the P_1Tone and Term, and connect all elements together.

2) Perform large-signal S-parameter simulations.

a) You will perform simulations at **source powers** of 0, 5 and 10 dBm.

b) After the first simulation (0 dBm) open the display window and create a pair of graphs, as shown in Figure 3. Add a data marker at 2 GHz. Your results should match the 'typical' results shown in the figure.

c) Perform the simulations at 5 and 10 dBm drive levels and fill in the corresponding spots in Table 1.

   i) Using the results at the 5 dBm drive level, determine (or extract) values for the diode junction resistance and capacitance (R_j and C_j, respectively, in Figure 1). You can assume the series resistance (R_s) is 5 Ohms.

      (1) Simulated value for Rj = _____

      (2) Simulated value for Cj = _____

   ii) Referring to the class notes, what typical range of values would we expect to find for these parameters?

      (1) Expected range of values for Rj = _____

      (2) Expected range of values for Cj = _____

Table 1. Large-signal simulation results for the schematic in Figure 2 at 2 GHz.

Port 2 Impedance (Ω)	P_1Tone Power Level (dBm)	S11 (dB)	Re{Zin} (Ω)	Im{Zin} (Ω)
50	0			
50	5			
50	10			

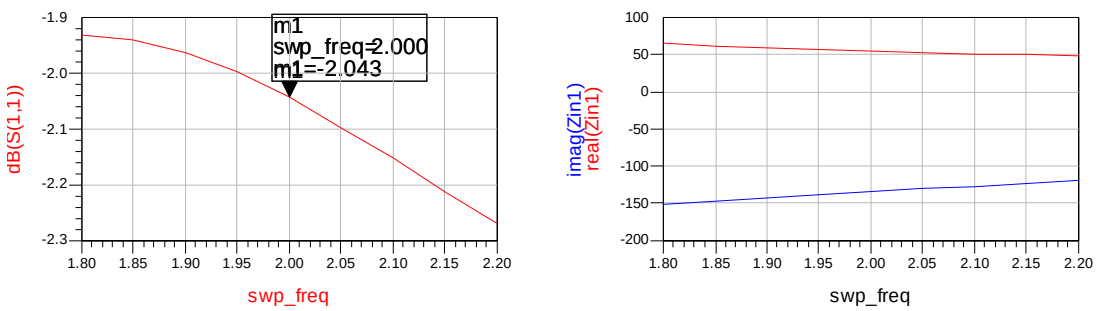

Figure 3. Typical plots for large-signal S11 and input impedance, using the schematic shown in Figure 2. The source power for these results was 0 dBm.

PART II. RF Impedance Matching Network for the Diode

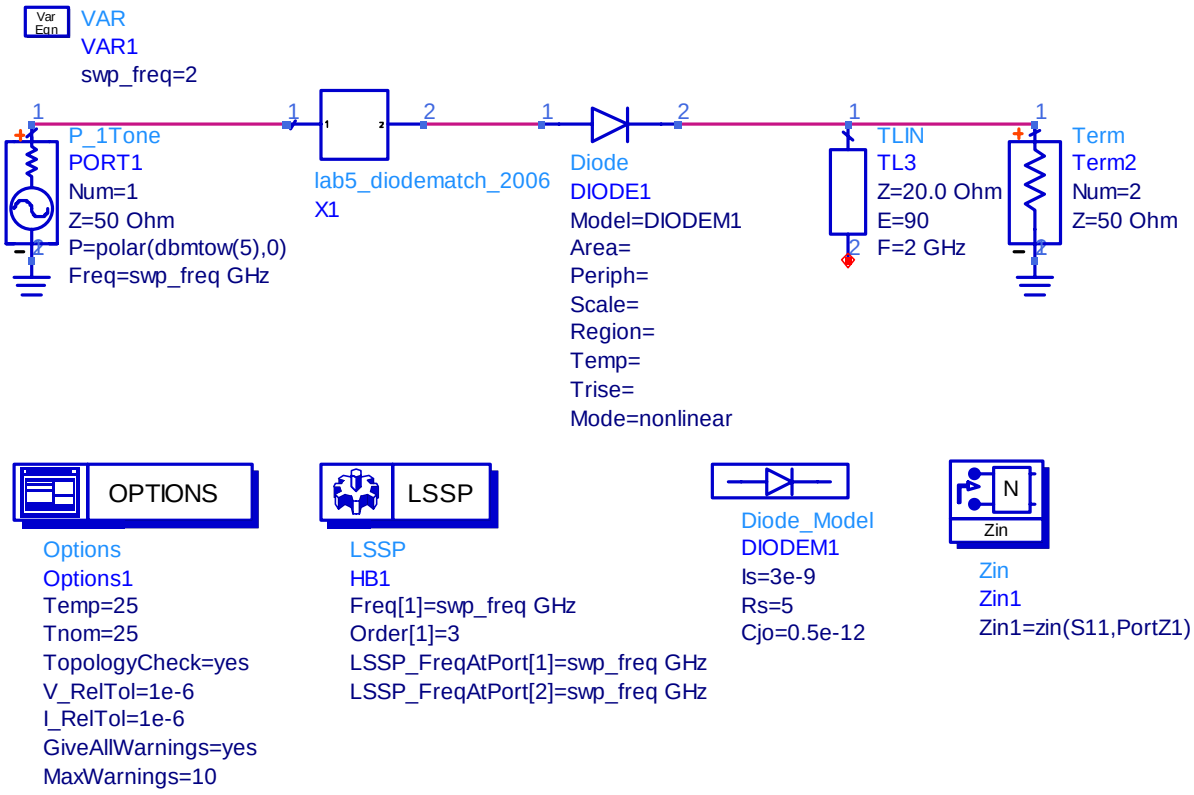

Figure 4. Schematic used for large-signal S-parameter simulation of the diode, including the (lumped element) RF matching network.

1) Using the simulated results from the previous section, design a two-element lumped matching network (using ideal elements) to match the input impedance (at 2 GHz) to 50 Ω. Use the values corresponding to a source power level of **5 dBm**.

2) Draw a sketch of your matching network below, and indicate the values of the elements.

3) Generate a schematic of the matching network (using ports, not terminations) and add a reference to this circuit from the higher-level schematic (see Figure 4). You may want to save the "higher-level" schematic to a new filename, in case you need to repeat any simulations from the previous section.

4) Perform large-signal simulations to test the effectiveness of your matching network.

   a) First perform simulations at source power levels of 0, 5 and 10 dBm. After the first simulation, open the display window and create a pair of graphs similar to those from the previous section. Fill in the corresponding spots in Table 2.

   b) Typical results at a source power level of 5 dBm are shown in Figure 5.

   c) OBTAIN A PRINTOUT OF THE GRAPHS OF YOUR RESULTS AT THE **5 DBM** DRIVE LEVEL. LABEL THE GRAPH "LAB 5 – DIODE MATCH RESULTS"

Table 2. Large-signal simulation results for the schematic in Figure 4 at 2 GHz.

Port 2 Impedance (Ω)	P_1Tone Power Level (dBm)	S11 (dB)	Re{Zin} (Ω)	Im{Zin} (Ω)
50	0			
50	5			
50	10			

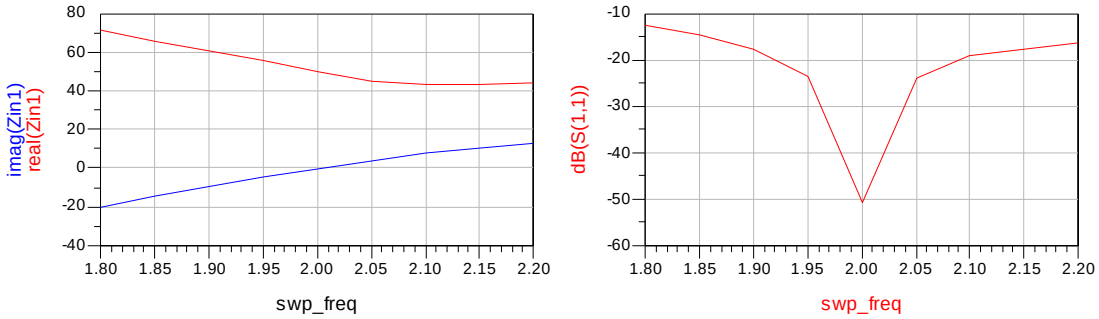

Figure 5. Typical plots for large-signal S11 and input impedance, using the schematic shown in Figure 4. The source power for these results was 5 dBm

Laboratory Reporting Requirements

ONLY SUBMIT pages from this laboratory procedure that contain data tables or answers to questions, along with the requested plots. If you want to keep the procedure together for future reference, attach the complete forms to the BACK of the basic report. This will greatly simplify the grading process.

1) Your report should include the following:
   a) Completed answers to all questions, tables, etc. in the laboratory procedure.
   b) The plots LAB 5 – DIODE MATCH RESULTS